INSTITUTE OF AERONAUTICAL ENGINEERING

Dundigal, Hyderabad - 500 043

COMPUTER SCIENCE AND ENGINEERING

TUTORIAL QUESTION BANK

Course Name	:	**Computer Organization**
Course Code	:	A40506
Class	:	II B. Tech II Semester
Branch	:	Computer Science and Engineering
Year	:	2016 – 2017
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OBJECTIVES

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

Group - A (Short Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
	2 MARKS QUESTIONS		
	UNIT – I		
1	**Explain** the role of program counter in addressing modes?	Understand	1
2	**Discuss** the different types of addressing modes?	Understand	2
3	**Define** condition codes? Can a processor be designed without any condition codes?	Knowledge	2
4	**Explain** the four basic types of operations that need to be supported by an instruction set?	Understand	3
5	**Describe** the Auxiliary carry flag usage?	Understand	1
6	**Define** conditional code/ status registers in computer organization?	Knowledge	3
7	**Explain** load and store architecture in microprocessor?	Understand	1
8	**Discuss** data structures that can be best supported using (a) indirect addressing mode (b) indexed addressing mode?	Understand	2
9	**Discuss** in detail instruction formats with various examples?	Knowledge	2
10	**Explain** the functional units of a general computer?	Understand	1
11	**List** out the instruction formats for Motorola 68000?	Knowledge	3
12	**List** out the different computer instruction formats?	Knowledge	3
13	**Explain** different types of addressing modes in branch instructions?	Understand	2
14	**Explain** briefly the operation of 'load' in Pentium microprocessor?	Understand	3

S. No	Questions	Blooms Taxonomy Level	Course Outcome
15	**Discuss** the usage of MAR and MDR in computer organization?	Knowledge	1
16	**Discuss** about micro instruction sequence in fetch instruction cycle?	Understand	3
17	**Explain** Little endian and big endian scheme of instructions.	Understand	2
18	**Define** conditional branch in computer organization?	Knowledge	2
19	**Differentiate** different architectures in computer organizations?	Knowledge	1
20	**Differentiate** hardwired control unit and micro programmed control unit with an example?	Knowledge	3
	UNIT - II		
1	**Distinguish** between memory mapped I/O and I/O mapped I/O?	Apply	6
2	**Distinguish** between a synchronous and an asynchronous data transfer mechanisms?	Apply	4
3	**Explain** a procedure to handle an interrupt?	Understand	3
4	**Differentiate** synchronous and asynchronous communication?	Understand	4
5	**Discuss** how DMA have priority over the CPU while memory transfer in CPU?	Understand	8
6	**Discuss** memory mapped I/O in computer organization?	Understand	6
7	**Explain** different hazards in pipeline concept while an instruction is transferd?	Understand	5
8	**Define** different factors considered while designing an I/O subsystem?	Knowledge	6
9	**List** the different methods used for handling the situation when multiple Interrupts occur?	Knowledge	3
10	**Discuss** the need of interrupt controller while instructions are executed?	Understand	3
11	**Explain** DMA operation? State its advantages?	Understand	7
12	**List** out the major functions of I/O system?	Knowledge	6
13	**Define** a port? Explain various types of ports available?	Knowledge	1
14	**Explain** the performance consideration in pipeline format?	Knowledge	8
15	**Define** intra segment and inter segment program control transfer in computer organization? (near and far pointer concept)	Knowledge	5
16	**Explain** the program-controlled I/O with an example?	Understand	7
17	**Discuss** interrupt masks provided in any processor?	Understand	3
18	**Define** the necessity and advantage of multiplexing the address and data bus?	Knowledge	6
19	**Discuss** the necessity of an interface in memory organization?	Understand	8
20	**Define** modes of data transfer in memory organization?	Knowledge	8
21	**Define** synchronous bus with read and write cycles?	Knowledge	4
22	**Define** asynchronous bus with read and write cycles?	Knowledge	4
23	**Explain** a privileged instruction set in memory?	Understand	2
24	**Discuss** the usage of an I/O controller. In memory organization?	Understand	4
25	**Explain** strobe control in asynchronous data transfer along with hand shaking problem?	Understand	3
	UNIT - III		
1	**Distinguish** between the write-through and write-back policies pointing out their merits and demerits?	Apply	8
2	**Define** the virtual memory organization and explain briefly?	Knowledge	10
3	**Explain** cache memory to reduce the execution time?	Understand	9
4	**Define** CPU registers, Main memory, Secondary memory and cache memory?	Knowledge	8
5	**List** the various types of semiconductor RAMs?	Knowledge	9
6	**Define** Random Access Memory and types of RAMs present?	Knowledge	9
7	**Explain** the necessary for memory hierarchy?	Understand	8
8	**Define** HIT and MISS ratio in memory with an example?	Knowledge	9
9	**Differentiate** SRAM and DRAM?	Understand	9
10	**List** out two kinds of address locality of reference in cache memory?	Knowledge	8

S. No	Questions	Blooms Taxonomy Level	Course Outcome
11	**List** out the two parameters for performance of a computer system?	Knowledge	2
12	**State** the differences between static and dynamic memories?	Knowledge	9
13	**Define** virtual or logical address?	Knowledge	8
14	**Define** cache memory? Explain how it is used to reduce the execution time?	Knowledge	9
15	**Explain** the mapping procedures adopted in the organization of a Cache Memory?	Understand	8
16	**Discuss** the function of a TLB? (Translation Look-aside Buffer)	Understand	11
17	**Differentiate** volatile and non volatile memory organization?	Knowledge	9
18	**Discuss** the multilevel hierarchy of storage devices?	Understand	8
19	**Explain** memory management unit (MMU)?	Understand	11
20	**Discuss** the enhancements used in the memory management?	Understand	8
21	**List** the factors that determine the storage device performance?	Knowledge	8
22	**Define** locality of reference? What are its types of locality of reference?	Knowledge	11
23	**Explain** basic concept of virtual memory technique?	Understand	10
24	**Define** Memory Access Time?	Knowledge	8
	UNIT - IV		
1	**List** out the major features of 8086 Microprocessors?	Knowledge	12
2	**Discuss** the significance of flags in flag register in 8086?	Understand	13
3	**Explain** how physical address is generated in 8086?	Understand	14
4	**Explain** the advantage of using memory segmentation?	Understand	14
5	**Discuss** how queue, speed up processing?	Understand	13
6	**Explain** about index registers?	Understand	13
7	**Classify** the usage of SI and DI registers?	Apply	13
8	**Describe** the functions of BIU?	Understand	13
9	**Explain** about timing and control unit in 8086?	Understand	13
10	**List** out the sequence of signals that occurs on address bus and data bus when microprocessor fetches an instruction?	Knowledge	12
11	**Explain** why 8086 internal architecture is divided into BIU and EU? Discuss the A-bus, B-bus and C- bus and their use?	Understand	12
12	**List** the internal registers in 8086 Microprocessor?	Knowledge	13
13	**Explain** the advantages of pipelining?	Understand	12
14	**Calculate** physical address using base and offset addresses in 8086?	Understand	14
15	**Discuss** the function of S_3 and S_4 Status signal of 8080 microprocessor?	Understand	14
16	**Explain** the roles of pins TEST, LOCK. With examples?	Understand	13
17	**Describe** how do you configure 8086 into minimum and maximum modes?	Understand	13
18	**Illustrate** the function of the *BHE* and ALE signals in 8086?	Apply	13
19	**Explain** which are the pins of 8086 that are to be connected to 8087 and explain their functions?	Understand	13
20	**Define** microprocessors and evolution of microprocessors?	Understand	12
21	**Classify** the functions of bus interface unit (BIU) in 8086?	Apply	13
22	**Analyze** the significance of *LOCK* signal in 8086?	Apply	13
23	**Define** pipelining concept and explain its working?	Understand	13
24	**Explain** the function of a segment register in 8086?	Understand	13
25	**Classify** various operating modes does 8086 with examples?	Apply	15
26	**Differentiate** the relation between 8086 processor frequency & crystal frequency?	Apply	14
27	**Explain** the purpose of MN/MX pin? Explain.	Understand	13
28	**Explain** how many 16 bit registers are available in 8086?	Understand	13
	UNIT - V		
1	**Define** relative memory addressing with an example?	Understand	
2	**Explain** the use of push and pop instruction in 8086 ?	Understand	

S. No	Questions	Blooms Taxonomy Level	Course Outcome
3	**Discuss** the function of stack pointer?	Understand	15
4	**Distinguish** between inter segment and intra segment jump instructions in 8086?	Apply	15
5	**Differentiate** between near CALL and far CALL instructions?	Apply	15
6	**Explain** about DOS function call?	Apply	16
7	**State** the difference between machine language and assembly language?	Apply	16
8	**Define** macro and procedure? Discuss the advantages of macro?	Understand	16
9	**Explain** the function of XLAT and CWD instructions in 8086?	Understand	16
10	**Explain** the two techniques to convert binary data to ASCII ?	Understand	16
11	**Explain** DAA, DAS instructions with examples?	Understand	17
12	**Explain** the instructions related to arithmetic and logical shift?.	Understand	17
13	**Describe** how REP instruction is used along with string instructions?	Understand	17
14	**Discuss** about cross-compiler?	Understand	17
15	**Differentiate** ENDS and ENDP directives?	Apply	16
16	**Explain** the operation performed by the 8086 when it executes the XLAT instruction. What is the use of XLAT?	Apply	16
17	**Explain** the function of the assembler directives BYTE PTR and WORD PTR.	Apply	16
18	**Define** non-Mask able interrupts?	Understand	17
19	**Differentiate** between RET and IRET instruction?	Apply	16
20	**Explain** IN and OUT instructions?	Understand	17
21	**Explain** ALIGN & ASSUME?	Understand	16
22	**Explain** PTR & GROUP?	Understand	16
23	**Discuss** how do you set and clear direction flag?	Understand	16
24	**Explain** how to set and clear trap flag?	Understand	17
25	**Explain** a program to check a number is odd or even number?	Knowledge	16

Group - II (Long Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
	UNIT – I		
1	**Define** an instruction format? Explain different types of instruction formats in detail.	Knowledge	1
2	**Explain** different types of addressing modes with Suitable examples?	Understand	2
3	**Define** an interrupt? Explain Types of interrupts?	Knowledge	3
4	**Illustrate** one-address and zero-address instruction formats, With Examples?	Apply	1
5	**Explain** i) Implied mode ii) Immediate Mode iii) Register Mode iv) Register indirect mode v) Direct addressing mode with Examples.	Understand	2
6	**Explain** different program control instructions in CPU?	Understand	3
7	**Discuss** status bit conditions with Diagram?	Understand	3
8	**Explain** conditional branch instructions?	Understand	2
9	**Compare** different instruction formats?	Understand	1
10	**Define** program interrupt? Explain External interrupts and internal interrupts.	Knowledge	3
11	**Explain** i) Indirect addressing Mode ii) Relative addressing Mode iii) Auto increment or auto decrement mode. Iv) Indexed addressing mode and Base register addressing mode.	Understand	2
	UNIT – II		
1	**Explain** the DMA transfer technique with the block diagram?	Understand	7
2	**Describe** input-output-processor (IOP) Organization in detail?	Understand	6
3	**Compare** I/O versus Memory bus?	Understand	6

S. No	Questions	Blooms Taxonomy Level	Course Outcome
4	**Explain** DMA Controller with the block diagram?	Understand	7
5	**Differentiate** isolated I/O and memory mapped I/O?	Understand	6
6	**Discuss** Strobe Control method of Asynchronous data transfer technique?	Understand	4
7	**Explain** Asynchronous communication interface with diagram?	Understand	4
8	**Discuss** various techniques used for Modes of Transfer?	Understand	5
9	**Explain** 8089 Input-Output processor?	Understand	7
10	**Describe** asynchronous serial transfer?	Understand	4
11	**Discuss** Handshaking method of Asynchronous data transfer technique?	Understand	4
	UNIT - III		
1	**Explain** briefly about memory hierarchy?	Understand	8
2	**Discuss** RAM and ROM chips with diagrams?	Understand	9
3	**State** and Explain virtual memory organization technique?	Remember	10
4	**Describe** in detail about associative memory?	Remember	8
5	**Define** cache memory? Explain Associative mapping technique?.	Remember	11
6	**Define** a mapping function? Explain Set-Associative mapping technique?	Remember	11
7	**Define** virtual memory? Discuss Address mapping using pages in virtual memory?	Remember	10
8	**Explain** i) ROM ii) PROM iii)EPROM iv)EEPROM.	Understand	9
9	**Explain** i) Write through policy ii) write back policy iii) Hit and Miss ratio.	Understand	11
10	**Explain** virtual memory Address translation?	Understand	10
11	**Explain** briefly about Memory connection to CPU?	Understand	7
	UNIT – IV		
1	**Explain** the various addressing modes of 8086 with examples?	Understand	15
2	**Explain** difference between 8086 and 8088?	Apply	12
3	**Explain** what are the GPR & SPR registers in 8086?	Understand	13
4	**Classify** flag register in 8086 and explain flag instruction set?	Apply	13
5	**Distinguish** between min mode and max mode of 8086?	Apply	13
6	**Explain** the functional block diagram of 8086and write about the functions of each block?	Understand	13
7	**Differentiate** between physical address, effective address and offset address?	Apply	14
8	**Explain** with example how physical address is generated?	Understand	14
9	**Discuss** the addressing modes provided by 8086with examples?	Understand	15
10	**Describe** and explain the minimum mode configuration of 8086 with read and write cycles of timing diagram?	Apply	13
11	**Describe** pin diagram of 8086 and explain each pin?	Apply	13
	UNIT - V		
1	**Discuss** the instructions formats of 8086 with examples?	Understand	16
2	**Describe** the following instructions with examples i)IMUL ii) XLATE iii) XCHG iv) MOVSB	Understand	17
3	**Explain** Arithmetic instruction set of 8086 with examples?	Understand	16
4	**Explain** data transfer instructions of 8086 with examples?	Understand	16
5	**Distinguish** macros & procedures?	Understand	16
6	**Explain** short notes on JUMP instructions with examples?	Understand	17
7	**Explain** the following instructions i). WAIT ii). HLT iii). ESC iv). NOP.	Understand	17
8	**Explain** If AL contains A0H, what happens when the instruction CBW is executed?	Understand	17
9	**Explain** the uses of Shift & rotate instructions?	Understand	16
10	**Differentiate** jump & loop instructions?	Apply	16
11	**Explain** short notes on string instructions?	Understand	16
12	**Identify** the logical instructions available in 8086?	Understand	16

Group - III (Critical Thinking / Analytical Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
	UNIT – I		
1	**Calculate** how many one-address instructions can be formulated when A Computer has 32-bit instructions and 12-bit address with 250 two-address instructions?	Apply	1
2	**List** a program to evaluate the arithmetic statement. X= A [B+C (D+E)] Using Zero address instructions. F(G+H)	Knowledge	1
3	**Calculate** the number of times control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is a computational type requiring an operand from memory?	Apply	2
4	**Calculate** the address field of an indexed addressing mode instruction to make it the same as a register indirect mode instruction?	Apply	3
5	**List** the basic differences between a branch instruction, a call subroutine instruction, and a program interrupt?	Knowledge	4
6	The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation field, a register address field, a mode field, and a memory address**. Determine** the instruction format and the number of bits in each field if the instruction is in one memory word?	Apply	8
7	The program in a computer compares two unsigned numbers A and B by performing a subtraction A-B and updating the status bits. Let A=01000001 and B=10000100, **Calculate** the values of Status bits C (borrow) and Z?	Apply	9
	UNIT - II		
1	**Indicate** whether the following constitute a control, status, or data transfer commands. a. Skip next instruction if flag is set. b. Seek a given record on a magnetic disk.	Understand	1
2	A CPU with a 20-MHZ clock is connected to a memory unit whose access time is 40 ns. **Formulate** a read and write timing diagrams using a READ strobe and a WRITE strobe, Include the address in the timing diagram.	Apply	4
3	**Calculate** the minimum number of bits that a frame must have in the bit-oriented protocol?	Apply	6
4	**Calculate** the number of characters per second can be transmitted over 1200-baud line in each of the following modes? a. Synchronous serial transmission. b. Asynchronous serial transmission with two stop bits.	Apply	4
5	In most computers an interrupt is recognized only after the execution of the current instruction. Consider the possibility of acknowledging the interrupt at any time during the execution of the instruction. **Discuss** the difficulty that may arise?	Understand	1
6	A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second**. Calculate** how much the CPU be slowed down because of the DMA transfer?	Apply	11
7	**Analyze** how DMA interrupt have priority over the processor interrupt when both interrupts occur simultaneously?	Apply	10
	UNIT – III		
1	A RAM chip has a capacity of 1024 words of 8 bits each (1K × 8). **Calculate** the number of 2 × 4 decoders with enable line needed to construct a 16K × 16 RAM	Apply	9

S. No	Questions	Blooms Taxonomy Level	Course Outcome
	from 1K × 8 RAM?		
2	**Calculate** The amount of ROM needed to implement a 4 bit multiplier?	Apply	9
3	A computer has a 256 K Byte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit**. Calculate** the number of bits in the tag field of an address?	Apply	10
4	A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. **Calculate** The number of bits for the TAG field?	Apply	11
5	In a k-way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set (s+1). The main memory blocks are numbered 0 onwards. **Calculate** The main memory block numbered j must be mapped to any one of the cache lines from?	Apply	11
6	Consider two cache organizations: The first one is 32 KB 2-way set associative with 32-byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has a latency of 0.6 ns while a k bit comparator has a latency of k/10 ns. The hit latency of the set associative organization is h1 while that of the direct mapped one is h2. **Calculate** The value of h1?	Apply	11
7	In many computers the cache block size is in the range 32 to 128 bytes. Discuss the main advantages and disadvantages of making the size of the cache blocks larger or smaller?	Understand	8
8	An eight-way set-associative cache consists of a total of 256 blocks. The main memory contains 8192 blocks, each consisting of 128 words. 1. **Calculate** number of bits in the main memory address? 2. **Calculate** number of bits in the TAG, SET and WORD fields?	Apply	11
9	**Calculate** numbers of 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?	Apply	9
10	**Explain** how will you calculate time Tb to access a block of data in serial access memory?	Apply	9
11	**Calculate** the number of page faults using First In First out (FIFO) Page Replacement Algorithm for the following CPU References. 3 4 5 6 4 7 4 0 6 7 4 7 6 5 6 4 5 3 4 5 Assume Main Memory contains 4 frames.	Apply	10
12	**Calculate** the number of page faults using Least Recently used (LRU) Page Replacement Algorithm for the following CPU References. 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1 Assume Main Memory contains 3 frames.	Apply	**10**
	UNIT – IV		
1	**Explain** the loop instructions of 8086? Explain the use of DF flag in the execution of string instructions?	Understand	16
2	**Explain** common function signals of 8086?	Understand	13
3	**Explain** about HOLD response sequence?	Understand	13
4	**Explain** hardware and software, vectored and non-vectored, I/O and processor interrupt in 8086?	Understand	14
5	**Explain** the architecture of 8086 with BIU and EU units and implementation of pipelining and instruction queue techniques?	Understand	13
6	**Explain** how odd memory bank is accessed in 8086?	Understand	12
7	**Explain** segmentation of memory in 8086?	Understand	14

S. No	Questions	Blooms Taxonomy Level	Course Outcome
	UNIT - V		
1	**Describe** an assembly language program to find sum of squares?	Understand	17
2	**Explain** a program sequence thatcompares thefirst 10 bytes beginning atCHAR_1with the first10bytes beginning at CHAR_2 and branches toMATCH. If they are equal, but otherwise continues in sequence	Understand	17
3	**Describe** program sequences that will perform the followingoperations ontwodigit packed BCD number. a. A=B+(C-6) b. A=(X+W) – (Z– (U*5))	Apply	17
4	**Describe** a program to read ASCII code after a strobe signal is sent from a Keyboard?	Apply	17
5	**Describe** a program to add a profit factor to each element in a cost array and puts the result in a prices array?	Apply	16
6	**Identify** the errors in the following instructions or groups of instructions. Loop: MOV BL,72H DEC BL JNZ loop	Understand	17

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