INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Name	:	**Computer Organization and Operating Systems**
Course Code	:	A505166
Class	:	III B. Tech I Semester
Branch	:	Electronics and Communication Engineering
Year	:	2017 – 2018
Course Faculty	:	Mr. CH.Srikanth, Ms. A Swapna, Ms. A Lakshmi Assistant Professor

OBJECTIVES

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

S. No	Questions	Blooms Taxonomy Level	Program Outcome
2 MARKS QUESTIONS			
UNIT – I			
1. Group - I (Short Answer Questions)			
1	**Explain** the role of program counter in Instruction execution?	Understand	1
2	**Describe** the basic functional units of a computer?	knowledge	1
3	**Define** memory access time.	Remember	2
4	**Explain** memory address register (MAR) and memory data register (MDR)?	Understand	1
5	**Define** two techniques used to increase the clock rate R?	Remember	2
6	**State** and Explain different types of addressing modes?	knowledge	2
7	**Describe** the IEEE standard for floating point numbers for single precision number.	knowledge	3
8	**Discuss** the single Bus architecture?	Understand	2
9	**Conver**t the following numbers with the indicated bases to decimal $(101101)_2$, $(736.4)_8$, (F3)16, and $(101001.1011)_2$?	comprehension	3

S. No	Questions	Blooms Taxonomy Level	Program Outcome
10	**Represen**t the number (+46.5)10 as a floating point binary number with 24 bits.	Analyze	2
11	**Classify** the Arithmetic Micro operations?	Understand	1
12	**Show** the diagram of one stage arithmetic logic shift unit?	Apply	2
13	**State** the role of the registers involved in instruction execution.	knowledge	4
14	**List** out differences between Multiprocessors and Multicomputer.	knowledge	3
15	**Explain** the three instruction code formats of a basic computer.	Understand	5
16	**Describe** the instruction cycle with the help of a neat diagram. Also draw the flow chart for the same.	knowledge	4
17	**State** the difference between arithmetic shift and logical shift.	knowledge	3
18	**Discuss** the different types of addressing modes?	Understand	2
19	**Define** condition codes? Can a processor be designed without any condition codes?	Remember	1
20	**Explain** the four basic types of operations that need to be supported by an instruction set?	Understand	3
21	**Define** conditional code/ status registers in computer organization?	Remember	2
22	**Discuss** data structures that can be best supported using (a) indirect addressing mode (b) indexed addressing mode?	Understand	2
23	**Explai**n the (r's) complement and (r-1)'s Complement.	Understand	3
24	**List** out the different computer instruction formats?	Knowledge	2
25	**Explain** Little endian and big endian scheme of instructions.	Understand	2
26	**Define** conditional branch in computer organization?	Remember	1
27	**Explain** the importance of RISC based System Architecture	Understand	5
28	**Explain** briefly about stored program organization with suitable example?	Understand	4
2. Group - II (Long Answer Questions)			
1	**Explain** the functional organization of a digital computer and explain the function of each element of a computer.	Understand	2
2	**Define** a digital computer? Discuss briefly on various types of computer.	Remember	1
3	**Illustrate** the diagram for connection between the processor and the memory and explain basic operational concepts of computer.	Apply	3
4	**Explain** about various buses such as internal, external, back plane, I/O System, address, data, synchronous	Understand	2
5	**Discuss** different Bus Structures in detail**.**	Understand	2
6	**Define** system software? Explain various functions of systems software.	Remember	3
7	**Explain** briefly about Basic Performance Equation.	Understand	2
8	**Explain** 2's Complement addition and Subtraction with numerical Examples.	Understand	2
9	The following transfer statements specify a memory. **Explain** the memory operation in each case. a) R<-M[AR] b) M[AR]<-R3 c) R<-	Understand	1

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	M[R5]		
10	**Discuss** briefly about Floating point Representation with Example.	Understand	5
11	**Draw** a Bus system for four registers using Multiplexers. Explain it in detail.	Knowledge	2
12	**Discuss** Three-state Bus Buffers with neat Diagram	Understand	1
13	**Explain** Binary Adder- Sub tractor with Diagram in detail.	Understand	3
14	**Draw** and explain 4-bit arithmetic circuit with neat diagram.	Knowledge	2
15	**Discuss** different applications of Logical micro-operations with Examples.	Understand	2
16	**Explain** different Shift Micro-operations with examples.	Understand	3
17	**Explain** the Arithmetic Logic Shift Unit with block diagram.		2
18	**List** and explain Memory reference instructions in detail.	Knowledge	3
19	**Explain** different Phases of Instruction Cycle with Examples.	Understand	2
20	**Discuss** briefly about Program control along with interrupt Cycle.	Understand	3
21	**Explain** the following related to Stack Organization. a)Register Stack b)Memory Stack	Understand	2
22	**Define** an instruction format? Explain different types of instruction formats in detail	Remember	1
23	**Explain** different types of addressing modes with Suitable examples	Understand	2
24	**Show** how can the following operation be performed using: a- three address instruction b- two address instruction c- one address instruction d- zero address instruction X = (A + B) * (C + D)	Application	4
25	**List** and explain different Data Transfer instructions.	Knowledge	2
26	**Specify** few memory reference-instructions.		3
27	**List** and explain Different Data manipulation instructions.	Knowledge	2
28	**Define** Condition-code bits**? Explain** status bit conditions with neat Diagram?	Remember	3
29	**List** and explain conditional branch instructions?	Knowledge	2
30	**Define** program interrupt? Explain External interrupts and internal interrupts.	Remember	1
31	**Explain** briefly about RISC architecture**.**	Understand	2
32	**Compare** the RISC and CISC architecture		4
33	**Discuss** the basic differences between a branch instruction, a call subroutine instruction, and program interrupt?	Understand	2

3. Group - III (Analytical Questions)			
1	**Illustrate** the signed magnitude, signed 1's complement, signed 2's complement for the decimal number -14.	Apply	5
2	**Convert** the following decimal numbers with the indicated bases to decimal. **a)** $(12121)_3$ b) $(4310)_5$ c) $(50)_7$ d) $(198)_{12}$	Understand	4
3	**Calculate** the subtraction with the following unsigned decimal numbers by taking the 10's complement of the subtrahend. 123900;090657:100000;000000	Apply	3
4	**Calculate** the arithmetic operations (+42) + (-13) and (-42) – (-13) in binary using signed 2's complement representation for negative numbers.	Apply	5
5	**Calculate the** arithmetic operations (+70) + (+80) and (-70) + (-80) with binary numbers in signed 2's complement representation. Use eight bits to accommodate each number together with its sign. Show	Apply	4

	that overflow Occurs in both cases.		
6	**Show** the number $(+46.5)_{10}$ as a floating-point binary number with 24 bits.	Apply	1
7	A 36-bit floating-point binary number has eight bits plus sign for the exponent and 26 bits plus sign for the mantissa. The mantissa is a normalized fraction. Numbers in the mantissa and exponent are in signed-magnitude representation. **Calculate** the largest and smallest positive quantities that can be represented, excluding zero.	Apply	1
8	Register A holds the 8 bit binary number 110111001. **Determine** the B operand and the logic micro operation to be performed in order to change the value in A to : a) 01101101 b) 11111101	Evaluate	2
9	Starting from an initial value of R=11011101, **Determine** the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by logical right and a circular shift left.	Evaluate	1
10	**Calculate** the following conditional control statement by two register transfer statements with control functions. If (p=1) then (R1← R2) else if (Q=1) then (R1←R3)	Apply	2
11	Register A holds the 4-bit binary number 1010 and Register B holds 4-bit binary number 1100. **Calculate** the A value by performing the following logical micro operations. a) selective-set b)mask c)selective- clear d)insert	Apply	2
12	An 8-bit register contains the binary value 10011100.Determine the register value after an arithmetic shift right? Starting from the initial number 10011100, **Determine** the register value after an arithmetic shift left,and state whether there is an overflow.	Evaluate	3
13	**Calculate** how many one-address instructions can be formulated when A Computer has 32-bit instructions and 12-bit address with 250 two-address instructions?	Apply	2
14	**List** a program to evaluate the arithmetic statement. $X= A [B+C (D+E)] \overline{F(G+H)}$ Using Zero address instructions.	Knowledge	3
15	**Calculate** the number of times control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is a computational type requiring an operand from memory?	Apply	2
16	**Calculat**e the address field of an indexed addressing mode instruction to make it the same as a register indirect mode instruction?	Apply	2
17	**List** the basic differences between a branch instruction, a call subroutine instruction, and a program interrupt?		3
18	The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation field, a register address field, a mode field, and a memory address**.** **Determine** the instruction format and the number of bits in each field if the instruction is in one memory word?	Evaluate	2
19	The program in a computer compares two unsigned numbers A and B by performing a subtraction A-B and updating the status bits. Let A=01000001 and B=10000100, **Calculate** the values of Status bits C (borrow) and Z?	Apply	3
20	A computer uses a memory unit with 256 words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. a. **Determine** how many bits are there in the operation code,the register code part and the address part b. **Draw** the instruction word format and indicate the number of bits in each part. c. **Determine** how many bits are there in the data and address inputs of	Evaluate	2

	the memory.		

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	UNIT – II		
	1. Group - I (Short Answer Questions)		
1	**Describe** the two approaches used for generating the control signals in proper sequence.	Knowledge	5
2	**Define** the following: (a) Micro-operation (b) Micro-instruction (c) Micro-program (d) Micro-code.	Remember	5
3	**Explain** the factors to determine the control signals?	Understand	5
4	**Discuss** the features of the hardwired control?	Understand	4
5	**Define** micro programmed control?	Remember	3
6	**Explain** control word?	Understand	5
7	**Define** micro routine and microinstruction.	Remember	4
8	**Differentiate** hardwired control and micro-programmed control.	Understand	3
9	**Define** control store?	Remember	4
10	**Explain** the drawback of micro programmed control?	Understand	6
11	**Discuss** the drawback of assigning one bit position to each control signals?	Understand	7
12	**Explain** the drawback of micro programmed control?	Understand	2
13	**Define** Memory Access time.	Remember	2
14	**Explain** the Formula for the average access time experienced by the processor in a system with two levels of catches.	Understand	1
15	**Explain** the following terms. i. Hit rate and ii. Miss penalty.	Understand	5
16	**Distinguish** between the write-through and write-back policies pointing out their merits and demerits	Apply	4
17	**Define** the virtual memory organization and explain briefly?	Apply	3
18	**Explain** cache memory to reduce the execution time?	Understand	2
19	**Define** CPU registers, Main memory, Secondary memory and cache memory?	Understand	5
20	**List** the various types of semiconductor RAMs?	Understand	5
21	**Define** Random Access Memory and types of RAMs present?	Remember	4
22	**Explain** the necessary for memory hierarchy?	Understand	2
23	**Define** HIT and MISS ratio in memory with an example?	Remember	3
24	**Differentiate** SRAM and DRAM?	Understand	7
25	**List** out two kinds of address locality of reference in cache memory?	Knowledge	6
26	**List** out the two parameters for performance of a computer system?	Knowledge	4
27	**State** the differences between static and dynamic memories?	Knowledge	5
28	**Define** virtual or logical address?	Remember	6
29	**Define** cache memory? Explain how it is used to reduce the execution time?	Remember	5
30	**Explain** the mapping procedures adopted in the organization of a Cache Memory?	Understand	6
31	**Discuss** the function of a TLB? (Translation Look-aside Buffer)	Understand	7
32	**Differentiate** volatile and non-volatile memory organization?	Remember	6
33	**Discuss** the multilevel hierarchy of storage devices?	Understand	4
34	**Explain** memory management unit (MMU)?	Understand	5
35	**Discuss** the enhancements used in the memory management?	Understand	3
36	**List** the factors that determine the storage device performance?	Knowledge	2
37	**Define** locality of reference? What are its types of locality of reference?	Remember	1
38	**Explain** basic concept of virtual memory technique?	Understand	6
39	**Calculate** maximum size of the memory that can be used in a 16-bit computer and 32 bit computer?	Apply	3

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	UNIT – II		
	2. Group - II (Long Answer Questions)		
1	**Define** Control memory? Explain Micro programmed Control Organization.	Remember	5
2	**Explain** operation of control unit of basic computer with diagram.	Understand	4
3	**Explain** briefly about Address Sequencing in control memory.	Understand	3
4	**Draw** and Explain the Microinstruction Format.		4
5	**Explain** the following related to Address Sequencing. a)Conditional branching b)Mapping of Instruction	Understand	6
6	**Explain** the Organization of Hardwired control in detail.	Understand	7
7	**List** the differences between hardwired control and micro programmed control.	Knowledge	2
8	**Explain** the Organization of Micro programmed control unit in detail.	Understand	2
9	**Explain** briefly about Micro-program Sequencer with diagram.	Understand	1
10	**Explain** the memory hierarchy with the reference of following metrics? a) Speed b) Cost c) Size	Understand	5
11	**Describe** Internal organization of memory chips in detail.	Knowledge	4
12	**Distinguish** between static and dynamic Memories pointing out their Merits and Demerits.	Analyze	3
13	**Explain** Read-Only Memories in detail.	Understand	2
14	**Explain** organization of a 1 K X 1 memory chip with neat diagram.	Understand	5
15	**Explain** i) ROM ii) PROM iii) EPROM iv) EEPROM.	Understand	5
16	**Discuss** Cache memories in detail		4
17	In many computers the cache block size is in the range of 32 to 128 bytes. **Discuss** the main advantages and disadvantage of making the size of cache blocks large or smaller?	Understand	3
18	**Define** a mapping function? Explain Associative mapping technique with its advantages and disadvantages?	Remember	4
19	**Explain** the following Cache Mapping Techniques (a) Direct Mapping (b) Set Associative Mapping.	Understand	6
20	**Distinguish between** write through write back policies pointing out their Merits and Demerits.	Analyze	7
21	**Explain** briefly about a) Hit Rate b) Miss Penalty with Examples.	Understand	6
22	**State** and Explain virtual memory organization technique with Diagram?	Knowledge	5
23	**Define** virtual memory? Explain with a diagram how virtual address can be mapped in to physical address using paging.	Remember	5
24	**Discuss** different RAID levels in detail with Diagrams	Understand	5
25	**Define** Page-fault? Explain the following page replacement algorithms with Examples a)FIFO b)LRU	Knowledge	4
26	**Explain** different Secondary Storage Devices with necessary Diagrams.	Understand	3
27	**Discuss** different RAID levels with Necessary Examples.	Understand	5

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	UNIT – II		
	3. Group - III (Analytical Questions)		
1	**Explain** how the mapping from and instruction code to a micro instruction address can be done by means of a Read-only memory	Understand	3
2	**Show** how a 9 bit micro operation field in a micro instruction can be divided into subfields to specify 46 micro operations. How many micro operations can be specified in one micro instruction.	Apply	5
3	A computer has 16registers, an ALU with 32 operations and a shifter with 8 operations, all connected to a common bus system a)**Formulate** a control word for a micro operation b) **Calculate** the number of bits in each field of the control word and give a general encoding scheme. c)**Show** the bits of the control word that specify the micro operation R4→R5+R6	Apply	4
4	A RAM chip has a capacity of 1024 words of 8 bits each (1K × 8). **Calculate** the number of 2 × 4 decoders with enable line needed to construct a 16K × 16 RAM from 1K × 8 RAM?	Apply	3
5	**Calculate** The amount of ROM needed to implement a 4 bit multiplier?	Apply	4
6	A computer has a 256 K Byte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit**.** **Calculate** the number of bits in the tag field of an address?	Apply	6
7	A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. **Calculate** The number of bits for the TAG field?	Apply	7
8	In a k-way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set (s+1). The main memory blocks are numbered 0 onwards. **Calculate** The main memory block numbered j must be mapped to any one of the cache lines from?	Apply	2
9	Consider two cache organizations: The first one is 32 KB 2-way set associative with 32-byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has a latency of 0.6 ns while a k bit comparator has a latency of k/10 ns. The hit latency of the set associative organization is h1 while that of the direct mapped one is h2. **Calculate** The value of h1?	Apply	2
10	In many computers the cache block size is in the range 32 to 128 bytes. **Discuss** the main advantages and disadvantages of making the size of the cache blocks larger or smaller?	Understand	6
11	An eight-way set-associative cache consists of a total of 256 blocks. The main memory contains 8192 blocks, each consisting of 128 words. 1. **Calculate** number of bits in the main memory address? 2. **Calculate** number of bits in the TAG, SET and WORD fields?	Apply	7
12	**Calculate** numbers of 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?	Apply	4
13	**Explain** how will you calculate time Tb to access a block of data in serial access memory?	Understand	6
14	**Calculate** the number of page faults using First In First out (FIFO) Page Replacement Algorithm for the following CPU References. 3 4 5 6 4 7 4 0 6 7 4 7 6 5 6 4 5 3 4 510 Assume Main Memory contains 4 frames.	Apply	7

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	UNIT - III		
1. Group - I (Short Answer Questions)			
1	**Define** an I/O Interface?	Remember	7
2	**Describe** the factors considered in designing an I/O subsystem?	Knowledge	6
3	**Explain** Direct Memory Access	Understand	4
4	**Explain** the different methods used for handling the situation when multiple interrupts occurs?	Understand	8
5	**Define** polling?	Remember	5
6	**Define** intra segment and inter segment program control transfer in computer organization? (near and far pointer concept)	Remember	5
7	**Discuss** the need of interrupt controller?	Understand	6
8	**List** the two independent mechanisms for controlling interrupt request?	Knowledge	4
9	**Define** vectored interrupts?	Remember	7
10	**Distinguish** between memory mapped I/O and I/O mapped I/O?	Apply	9
11	**Define** bus.	Remember	4
12	**Discuss** the necessity of an interface in memory organization?	Understand	6
13	**Define** synchronous bus.	Remember	2
14	**Discuss** the usage of an I/O controller. In memory organization?	Understand	3
15	**Define** asynchronous bus.	Remember	4
16	**State** and explain memory mapped I/O?	knowledge	7
17	**Explain** program-controlled I/O?	Understand	5
18	**Explain** the performance consideration in pipeline format?	Understand	8
19	**Define** a privileged instruction?	Remember	4
20	**Discuss** bus arbitration?	Understand	3
21	**Define** port? What are the types of port available?	Remember	4
22	**Explain** PCI bus?	Understand	7
23	**Define** USB.	Remember	8
24	**Discuss** different objectives of USB?	Understand	9
25	**Distinguish** between a synchronous and an asynchronous data transfer mechanisms?	Apply	5
26	**Explain** a procedure to handle an interrupt?	Understand	5
27	**Define** DMA controller?	Remember	7
28	**Differentiate** synchronous and asynchronous communication?	Understand	6
29	**Discuss** how DMA have priority over the CPU while emory transfer in CPU?	Understand	7
30	**Discuss** memory mapped I/O in computer organization?	Understand	8
32	**Define** different factors considered while designing an I/O subsystem?	Remember	5
33	**Discuss** the need of interrupt controller while instructions are executed?	Understand	6
34	**Explain** DMA operation? State its advantages?	Understand	4
35	**List** out the major functions of I/O system?	Remember	3
36	**Define** a port? Explain various types of ports available?	Remember	9
37	**Explain** the program-controlled I/O with an example?	Understand	4
38	**Discuss** interrupt masks provided in any processor?	Understand	8
39	**Define** the necessity and advantage of multiplexing the address and data bus?	Remember	7
40	**Define** modes of data transfer in memory organization?	Remember	7
41	**Define** synchronous bus with read and write cycles?	Remember	5
42	**Define** asynchronous bus with read and write cycles?	Remember	9
43	**Explain** a privileged instruction set in memory?	Understand	7
44	**Explain** strobe control in asynchronous data transfer along with hand shaking problem?	Understand	5

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	UNIT - III		
	2. Group - II (Long Answer Questions)		
1	**Distinguish** between memory mapped I/O and I/O mapped I/O.	Analyze	6
2	**Differentiate** isolated I/O and memory mapped I/O?	Analyze	4
3	**Discuss** I/O interface in detail with example.	Understand	7
4	**Explain** Strobe Control method of Asynchronous data transfer technique.	Understand	9
5	**Describe** Asynchronous serial transfer in detail.	Knowledge	4
6	**Discuss** First-In, First-Out Buffer with neat diagram.	Understand	6
7	**Discuss** Handshaking method of Asynchronous data transfer technique?	Understand	2
8	**Explain** briefly about Asynchronous communication interface with diagram.	Understand	3
9	**Discuss** DMA transfer technique in detail with block diagram?	Understand	4
10	**Explain** the following a)CPU-IOP communication b)Daisy- Chaining priority c)Bit-oriented protocol	Understand	7
11	**Discuss** the Character-oriented Protocol with Example.	Understand	5
	Distinguish between programmed I/O and Interrupt initiated IO with example.	Analyze	8
12	**Discuss** the following a) Parallel priority Interrupt. b)Priority Encoder	Understand	4
13	**Explain** briefly about DMA Controller with block diagram	Understand	3
14	**Explain** the operation of input output processor (IOP) with an example.	Understand	4
15	**Explain** different modes of Data Transfer to and From Peripherals	Understand	7
16	**Explain** 8089 Input-Output processor with necessary Diagram.	Understand	8
17	**Discuss** briefly about PCI bus with diagram.	Understand	9
18	**Discuss** the following a) Interrupt-initiated I/O b) Interrupt Cycle	Understand	8
19	**Distinguish** between I/O Bus and Memory bus.	Analyze	4
20	**Discuss** USB Serial communication protocol in detail.	Understand	3
21	**Draw** and Explain the Connection of I/O bus to input-output devices		8
22	**Explain** briefly about Input-output Processor with Diagram.	Understand	4

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	UNIT-III		
	3. Group - III (Analytical Questions)		
1	**Indicate** whether the following constitute a control, status, or data transfer commands. a. Skip next instruction if flag is set. b. Seek a given record on a magnetic disk.	Understand	8
2	A CPU with a 20-MHZ clock is connected to a memory unit whose access time is 40 ns. **Formulate** a read and write timing diagrams using a READ strobe and a WRITE strobe, Include the address in the timing diagram.	Create	5
3	**Calculate** the minimum number of bits that a frame must have in the bit-oriented protocol?	Apply	5
4	**Calculate** the number of characters per second can be transmitted over 1200-baud line in each of the following modes? a. Synchronous serial transmission. b. Asynchronous serial transmission with two stop bits.	Apply	6

5	In most computers an interrupt is recognized only after the execution of the current instruction. Consider the possibility of acknowledging the interrupt at any time during the execution of the instruction. **Discuss** the difficulty that may arise?	Understand	4
6	A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second**. Calculate** how much the CPU be slowed down because of the DMA transfer?	Apply	7
7	**Analyze** how DMA interrupt have priority over the processor interrupt when both interrupts occur simultaneously?	Analyze	9
8	**Discuss** atleast six status conditions for the setting of individual bits in the status register of an Asynchronous communication interface?	Understand	4
9	**State** and explain the basic advantage of using interrupt initiated data transfer over transfer under programme control without an interrupt?	Knowledge	6
10	**Design** a parallel priority interrupt hardware for a system with eight interrupt sources.	Create	2
11	**Show** how the zero instruction works in the bit oriented protocol when a zero followed by the 10 bits that represent the binary equivalent of 1023 are transmitted **?**	Apply	3

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	UNIT – IV		
	1. Group - I (Short Answer Questions)		
1	**Define** Operating System? Explain the three main purposes of an operating system?	Remember	9
2	**Define** kernel? List at least two functions of the kernel.	Remember	11
3	**Define** thread? Explain about multithreading.	Remember	12
4	**Describe** the process state diagram	Knowledge	10
5	**Explain** the advantages of Multiprogramming	Understand	13
6	**State** the advantage of multiprocessor system	Knowledge	9
7	**Explain** the difference between multiprocessor and multiprocessing?	Understand	5
8	**Compare** user threads and kernel threads.	Analyze	11
9	**Discuss** the use of fork () and exec () system calls?	Understand	10
10	**Explain** the use of job queues, ready queues and device queues?	Understand	12
11	**State** and Explain advantages of context switch?	Knowledge	10
12	**Define** scheduler? List different types of Schedulers.	Remember	9
13	**Discuss** scheduling a process? What are the types of schedules available?	Understand	10
14	**Explain** about Multi-Threading Models.	Understand	11
15	**Discuss** various issues involved in implementing Inter process communication (IPC) in message passing system.	Understand	12
16	**Discuss** about Process concept and process scheduling	Understand	13
17	**Explain** the purpose of system calls? Discuss the types of system calls provided by a typical operating system.	Understand	10
18	**Differentiate** hard real system and soft real system?	Understand	13
19	**Explain** boot strap program? Where will it be stored?	Understand	12
20	**List** the difference between a trap and an interrupt? What is the use of each function?	Knowledge	11
21	**Define** dispatcher? List the Purposes of dispatcher.	Remember	10
22	**Define** logical address and physical address.	Remember	13
23	**Explain** logical address space and physical address space?	Understand	11
24	**Discuss** the main function of the memory-management unit?	Understand	12
25	**Explain** dynamic loading.	Understand	9
26	**Define** dynamic linking.	Remember	11

27	**Define** swapping technique.	Remember	13
28	**Explain** the common strategies to select a free hole from a set of available holes?	Understand	10
29	**Explain** the advantages of best fit	Understand	10
30	**List** the differences between internal and external fragmentation.	Knowledge	9
31	**Explain** the advantages of first fit?	Understand	10
32	**Explain** virtual memory?	Understand	11
33	**Discuss** the major problems to implement demand paging?	Understand	12
34	**Explain** the advantages of Demand paging?	Understand	13
35	Assume you have a page reference string for a process with m frames (initially all empty). The page reference string has length p with n distinct page numbers occurring in it. For any page-replacement algorithms, a) **State** lower bound on the number of page faults? b) **State** upper bound on the number of page faults?	Knowledge	10
36	**Discuss** pure demand paging?		13
37	**Explain** the main function of the memory-management unit?	Understand	12
38	**Define** effective access time.	Remember	11
39	**Discuss** the problems exists in contiguous memory allocation	Understand	10
40	**Define** secondary memory.	Remember	13
41	**Explain** the basic approach of page replacement?	Understand	11
42	**Discuss** the various page replacement algorithms used for page replacement?	Understand	12
43	**Explain** the major problems to implement demand paging?	Understand	9
44	**Define** a reference string?	Remember	10
45	**Explain** the advantages of Contiguous allocation?	Understand	9
46	**Differentiate** segmentation and paging technique?	Analyze	10
47	**Define** Paging.	Remember	11
48	**Define** Segmentation.	Remember	12
49	**Discuss** the two solutions for the problem of external fragmentation?	Understand	13
50	Define hashed page table and clustered page table.	Remember	10

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	UNIT – IV		
	2. Group - II (Long Answer Questions)		
1	**State** and explain the various types of computer systems.	Knowledge	11
2	a) **Define** an operating system? State and explain the basic functions or services of an operating system. b). **List** the differences between multiprogramming and Time-sharing systems.	Understand Knowledge	11
3	**Explain** how protection is provided for the hardware resources by the operating system.	Understand	10
4	**Describe** the system components of an operating system and explain them briefly.	Understand	12
5	**Describe** the operating system structures.	Knowledge	10
6	**Discuss** about the following structures of OS. a. Simple structures b. Layered approach c. Micro kernels	Understand	9
7	**Explain** briefly about System calls with Examples.	Understand	10
8	**Discuss** briefly about Swapping concept with necessary Examples.	Understand	11
9	**Describe** contiguous memory allocation concept with advantages and disadvantages.	Knowledge	12

10	**Compare** the main memory organization schemes of contiguous-memory allocation, segmentation, and paging with respect to the following issues: a. external fragmentation b. internal fragmentation c. ability to share code across processes	Understand	13
11	**Differentiate** between internal and external fragmentation**.** Which one occurs in paging scheme.	Understand	10
12	**Explain** briefly about Paging with neat diagram.	Understand	9
13	**Discuss** the following a)Hierarchical paging b)Inverted page Tables	Understand	10
14	**Draw** and explain the working procedure of paging hardware in detail.	Knowledge	11
15	**Explain** the basic concepts of segmentation with neat diagrams.	Understand	12
16	**Define** page fault? When does a page fault occur? Describe the action taken by OS when page fault occurs.	Remember	13
17	**State** and explain about Virtual memory concept with neat diagram.	Knowledge	10
18	**Differentiate** between paging and segmentation.	Understand	9
19	**Explain** briefly about performance of Demand paging with necessary Examples.	Understand	10
20	**Explain** the basic Scheme of page replacement and about the various page replacement strategies with examples.	Understand	11
21	Consider the following page-reference string: 1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6 **Calculate** How many page faults would occur for the following replacement algorithms, assuming frame size is 4.Remember that frames are initially empty. (i)LRU replacement (ii)FIFO replacement (iii)Optimal replacement	Apply	10
22	**Define** thrashing? Explain the different methods to avoid thrashing.	Remember	9
23	**Define** deadlock? What are the four conditions necessary for deadlock? How it can be prevented.	Remember	10
24	**Explain** briefly about resource allocation graph with examples.	Understand	11
25	**Explain** about the methods used to prevent deadlocks.	Understand	12
26	**Discuss** in detail about deadlock avoidance.	Understand	13
27	**Explain** the Banker's algorithm for deadlock avoidance with Example.	Understand	10
28	**Discuss** deadlock detection in detail.	Understand	9
29	**State** and explain the methods involved in recovery from deadlocks	Knowledge	10
30	Consider the following snapshot of a system: **Allocation** **Max** **Available** *A B C* *A B C* *A B C* P_0 0 1 0 0 0 0 0 0 0 P_1 2 0 0 2 0 2 P_2 3 0 3 0 0 0 P_3 2 1 1 1 0 0 P_4 0 0 2 0 0 2 Answer the following questions using the banker's algorithm: a. **Calculate** is the content of the matrix need? b. **Identify** the system in a safe state?	Apply	11

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	UNIT – IV		
	3. Group - III (Analytical Questions)		
1	**Discuss** briefly about the view of an OS as a Resource Manager	Understand	10
2	**Explain** how operating system services are provided by system calls.	Understand	13

3	**Explain** the main difficulty that a programmer must overcome in writing an operating system for a real-time environment.	Understand	9
4	**Discuss** how the distinction between kernel mode and user mode function does. as a rudimentary form of protection (security) system	Understand	10
5	Some early computers protected the operating system by placing it in a memory partition that could not be modified by either the user job or the operating system itself. **Describe** two difficulties that you think could arise with such a scheme.	Understand	13
6	Consider a system in which a program can be separated into two parts: code and data. The CPU knows whether it wants an instruction (instruction fetch) or data (data fetch or store). Therefore, two base–limit register pairs are provided: one for instructions and one for data. The instruction base–limit register pair is automatically read-only, so programs can be shared among different users. **Discuss** the advantages and disadvantages of this scheme	Understand	9
7	Most systems allow programs to allocate more memory to its address space during execution. Data allocated in the heap segments of programs is an example of such allocated memory. **Explain** what is required to support dynamic memory allocation in the following schemes. a. Contiguous-memory allocation b. Pure segmentation c. Pure paging.	Understand	5
8	Consider a paging system with the page table stored in memory. a. If a memory reference takes 200 nanoseconds, **Identify** how long does a paged memory reference take? b. If we add associative registers, and 75 percent of all page-table references are found in the associative registers, what is the effective memory reference time? (Assume that finding a page-table entry in the associative registers takes zero time, if the entry is there).	Knowledge	11
9	**Compare** the main memory organization schemes of contiguous-memory allocation, segmentation, and paging with respect to the following issues: a. external fragmentation b. internal fragmentation c. ability to share code across processes	Understand	10
10	Consider a logical address space of eight pages of 1024 words each, mapped onto a physical memory of 32 frames. a. **Calculate** how many bits are there in the logical address? b. **Calculate** how many bits are there in the physical address?	Apply	13
11	**Discuss** why are page sizes always powers of 2?	Understand	9
12	Given memory partitions of 100K, 500K, 200K, 300K, and 600K (in order), how would each of the First-fit, Best-fit, and Worst-fit algorithms place processes of 212K, 417K, 112K, and 426K (in order)? **Discuss** algorithm makes the most efficient use of memory?	Understand	5
13	Suppose we have a demand paged memory. The page table is held in registers. It takes 8 milliseconds to service a page fault if an empty frame is available or the replaced page is not modified and 20 milliseconds if the replaced page is modified. Memory access time is 100 nanoseconds. Assume that the page to be replaced is modified 70 percent of the time. **Calculate** the maximum acceptable page-fault rate for an effective access time of no more than 200 nanoseconds?	Apply	11
14	Why do you require page replacement? What are the various page replacement techniques available? **Explain** each for the following sequence of pages on demand for process execution and also identify which technique is best suitable for the sequence. 1, 2, 3, 4, 5, 3, 4, 1, 6, 7, 8, 7, 8, 9, 7, 8, 9, 5, 4, 5, 4,2	Understand	10

15	Sharing segments among processes without requiring the same segment number is possible in a dynamically linked segmentation system. a. **Define** a system that allows static linking and sharing of segments without requiring that the segment numbers be the same. b. **Describe** a paging scheme that allows pages to be shared without requiring that the page numbers be the same	Knowledge	12
16	Under what circumstances do page faults occur? **Describe** the actions taken by the operating system when a page fault occurs.	Knowledge	10
17	**Discuss** situations under which the least frequently used page replacement algorithm generates fewer page faults than the least recently used page-replacement algorithm. Also discuss under what circumstance the opposite holds.	Understand	9
18	Consider the following page-replacement algorithms. Rank these algorithms on a five-point scale from "bad" to "perfect" according to their page-fault rate. **Distinguish** those algorithms that suffer from Belady's anomaly from those that do not. a. LRU replacement b. FIFO replacement c. Optimal replacement	Understand	10
19	A certain computer provides its users with a virtual-memory space of 2^{32} bytes. The computer has 218 bytes of physical memory. The virtual memory is implemented by paging, and the page size is 4096 bytes. A user process generates the virtual address 11123456. **Explain** how the system establishes the corresponding physical location. Distinguish between software and hardware operations	Understand	11
20	**Compare** the circular-wait scheme with the deadlock-avoidance schemes(like the banker's algorithm) with respect to the following issues: a. Runtime overheads **b.** System throughput	Understand	12
S. No	**Questions**	**Blooms Taxonomy Level**	**Program Outcome**
21	Consider a system consisting of four resources of the same type that are shared by three processes, each of which needs at most two resources. **Show** that the system is deadlock-free	Apply	13
22	Consider a system consisting of *m* resources of the same type, being shared by *n* processes. Resources can be requested and released by processes only one at a time. **Show** that the system is deadlock free if the following two conditions hold: a. The maximum need of each process is between 1 and *m* resources *b.* The sum of all maximum needs is less than *m* + *n*	Apply	10
23	Consider the following snapshot of a system: **Allocation** **Max** **Available** *A B C D* *A B C D* *A B C D* P_0 0 0 1 2 0 0 1 2 1 5 2 0 P_1 1 0 0 0 1 7 5 0 P_2 1 3 5 4 2 3 5 6 P_3 0 6 3 2 0 6 5 2 P_4 0 0 1 4 0 6 5 6 Answer the following questions using the banker's algorithm: a. **Calculate** content of the matrix need? b. **Identify** whether the system in a safe state? c. If a request from process P_1 arrives for (0,4,2,0), **Describe** the request be granted immediately?	Apply	13
24	Can a system detect that some of its processes are starving? If you answer "yes," **Explain** how it can. If you answer "no," explain how the system can deal with the starvation problem.	Understand	12
25	Is it possible to have a deadlock involving only one single-threaded Process ? **Explain** your answer.	Understand	11

UNIT – V			
1. Group - I (Short Answer Questions)			
1	**Define** a file?	Remember	14
2	**List** the various file attributes.	Knowledge	13
3	**Discuss** the various file operations?	Understand	11
4	**Describe** the layout of a file system?	Knowledge	12
5	**State** the information associated with an open file?	Knowledge	14
6	**List** the different accessing methods of a file?	Knowledge	13
7	**Explain** the operations that can be performed on a directory?	Understand	12
8	**Explain** the most common schemes for defining the logical structure of a directory?	Understand	14
9	**Describe** the various layers of a file system?	Knowledge	13
10	**List** the structures used in file-system implementation?	Knowledge	10
11	**Explain** the functions of virtual file system (VFS)?	Understand	11
12	**Define** seek time and latency time.	Remember	14
13	**Discuss** the allocation methods of a disk space?	Understand	13
14	**Explain** the advantages of Contiguous allocation?	Understand	12
15	**Discuss** the drawbacks of contiguous allocation of disk space?	Understand	14
16	**Explain** the advantages of Linked allocation?	Understand	13
17	**Explain** the disadvantages of linked allocation?	Understand	12
18	**List** the advantages of Indexed allocation?	Knowledge	14
19	**Define** rotational latency and disk bandwidth.	Remember	11
20	**Discuss** how free-space is managed using bit vector implementation?	Understand	12
21	**Explain** the general model of a File System.	Understand	10
22	**Discuss** the inadequacies of simple file system.	Understand	12
23	**Explain** the most common schemes for defining the logical structure of a directory?	Understand	14
24	**Define** UFD and MFD	Remember	13
25	**List** the various layers of a file system?	Knowledge	12
26	**Explain** the structures used in file-system implementation?	Understand	14
27	**State** and explain how can the index blocks be implemented in the indexed allocation scheme?	Knowledge	11
28	**Define** rotational latency and disk bandwidth.	Remember	12

S. No	Questions	Blooms Taxonomy Level	Program Outcome
	UNIT – V		
	Group - II (Long Answer Questions)		
1	**Discuss** various file access methods in detail	Understand	14
2	**Explain** briefly about directory structure with diagrams	Understand	13
3	**Differentiate Sequential access and direct access with suitable examples**	Understand	12
4	**Discuss** File System implementation in detail with suitable diagrams	Understand	14
5	**Describe** the following most common schemes for defining the logical structure of a diagram **a)** Single-level directory **b)** Two-level directory	Knowledge	13
6	**Explain** the Banker's algorithm for deadlock avoidance with Example.	Understand	10
7	**Explain** briefly about Tree structured directories with diagram	Understand	11
8	**Define** mount point? Explain File system mounting in detail?	Knowledge	14
9	**Explain** briefly about Acyclic-Graph Directories structure with	Understand	13

	diagram		
10	**Explain** in detail about File sharing and protection?	Understand	12
11	**Define** Directory? Explain General Graph directory Structure in detail?	Knowledge	14
12	**Define** File system? Explain Layered File system in detail?	Knowledge	13
13	**Explain** briefly about virtual File system with diagram?	Understand	12
14	**Discuss** Contiguous File Allocation method with suitable examples?		14
15	**Define** Free-Space list? Explain different implementation methods for free space management?	Knowledge	11
16	**Explain** briefly about Linked File Allocation method with example?	Understand	12
17	**Distinguish** between Contiguous and linked File allocation methods?	Understand	10
18	**Discuss** Indexed File Allocation methods with suitable examples?	Knowledge	14
19	**Discuss** the following a)File attributes b)File types c)Internal File structure	Knowledge	13

S. No	Questions	Blooms Taxonomy Level	Program Outcome
UNIT – V			
3. Group - III (Analytical Questions)			
1	Consider a file system where a file can be deleted and its disk space Reclaimed while links to that file still exist. **Discuss** the problems may occur if a new file is created in the same storage area or with the same absolute path name? How can these problems be avoided?	Understand	14
2	**Explain** the advantages and disadvantages of recording the name of the creating program with the file's attributes (as is done in the Macintosh Operating System)?	Understand	13
3	Some systems automatically open a file when it is referenced for the first time, and close the file when the job terminates. **Discuss** the advantages and disadvantages of this scheme as compared to the more traditional one, where the user has to open and close the file explicitly.	Understand	12
4	In some systems, a subdirectory can be read and written by an Authorized user, just as ordinary files can be. a) **Describe** the protection problems that could arise. b) **Define** a scheme for dealing with each of these protection Problems.	Knowledge	14
5	**Describe** an example of an application that could benefit from operating system support for random access to indexed files	Knowledge	13
6	**Discuss** the merits and demerits of supporting links to files that cross mount points (that is, the file link refers to a file that is stored in a different volume).	Understand	10
7	Some systems provide file sharing by maintaining a single copy of a file; other systems maintain several copies, one for each of the users sharing the file**. Discuss** the relative merits of each approach.	Understand	11
8	Consider a file system that uses a modified contiguous-	Understand	14

	allocation scheme with support for extents. A file is a collection of extents, with each extent corresponding to a contiguous set of blocks. A key issue in such systems is the degree of variability in the size of the extents. **Explain** the advantages and disadvantages of the following schemes: a. All extents are of the same size, and the size is predetermined. b. Extents can be of any size and are allocated dynamically. c. Extents can be of a few fixed sizes, and these sizes are predetermined.		
9	**Explain** the advantages of the variation of linked allocation that uses FAT to chain together the blocks of a file?	Understand	12
10	Consider a system where free space is kept in a free-space list. a. Suppose that the pointer to the free-space list is lost. Can the System reconstructs the free-space list? **Explain** your answer. b. Consider a file system similar to the one used by UNIX with Indexed allocation. How many disk I/O operations might be Required to read the contents of a small local file at */a/b/c*? Assume That none of the disk blocks is currently being cached. c. Suggest a scheme to ensure that the pointer is never lost as a Result of memory failure.	Understand	14
11	Consider a file system on a disk that has both logical and physical block sizes of 512 bytes. Assume that the information about each file is already in memory. For each of the three allocation strategies (contiguous, linked, and indexed), answer these questions a. **Identify** how the logical-to-physical address mapping accomplished In this system? (For the indexed allocation, assume that a file is Always less than 512 blocks long.) b. If we are currently at logical block 10 (the last block accessed was block 10) and want to access logical block 4, how many physical blocks must be read from the disk?	**Knowledge**	13

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