INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

Course Name	**:**	**DIGITAL DESIGN USING VERILOG HDL**
Course Code	**:**	A40410
Class	**:**	II B. Tech II Semester
Branch	**:**	Electronics and Communication Engineering
Year	**:**	2016 – 2017
Course Faculty	**:**	Mr. Khalandar Basha, Mr. K. Arun Sai, Mr. K Sudhakar Reddy, Mr. N Nagaraju

OBJECTIVES:

Designing digital circuits at behavioral and RTL modeling of digital circuits using verilog HDL. verifying these models, and synthesizing RTL models to standard cell libraries and FPGAs.

Students gain practical experience by designing, modeling, implementing and verifying several digital circuits. This course aims provide students with the Understand of different technologies related to HDLs, constructs, compile and execute Verilog HDL programs using provided software tools. Design digital components and circuits that are testable, reusable and synthesizable.

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	UNIT - I **INTRODUCTION TO VERILOG HDL**		
	Part – A (Short Answer Questions)		
1	Define verilog HDL?	Understanding	1
2	List levels of design description in verilog HDL?	Analyze	1
3	Describe is concurrency?	Analyze	1
4	What is simulation and synthesis?	Analyze	1
5	What is functional verification?	Remember	1
6	What are system tasks?	Understand	1
7	Write short notes on programming language interface (PLI).	Remember	1
8	What is module?	Understand	1
9	What is a simulation and synthesis tool?	Remember	1
10	What is test bench?	Understand	1
11	Define keywords and identifiers?	Remember	1
12	What are white space characters?	Remember	1
13	Define comments and numbers?	Understand	1
14	Define strings and logic values?	Remember	1
15	What is a data types? And what are those?	Understand	1
16	Define scalars and vectors?	Evaluate	1
17	Define parameters and memory operators?	Evaluate	1
	Part – B (Long Answer Questions)		
1	Write short note on “Verilog as HDL”	Apply	1
2	Discuss Level of design description.	Apply	2

3	Explain top-down design methodology with example.	Understand	2
4	Write short notes on, (a) Concurrency (b) Functional verification	Knowledge	1
5	Define the following terms relevant to Verilog HDL, (a) Simulation versus synthesis. (b) PLI (c) System tasks.	Analyze	2
6	what are the system tasks available in Verilog for making and controlling simulation ?	Apply	1
7	Explain about, (a) Display tasks (b) Strobe tasks (c) Monitor tasks with examples.	Understand	1
8	Define the following terms relevant to Verilog HDL. (a) Module (b) Test bench.	Understand	1
9	Write a syntax functions and tasks with one example.	Apply	1
10	Write about $readmemb with example.	Analyze	2
11	Write value change dump file.	Understand	1
12	Explain the synthesis procedure in Verilog HDL.	Understand	1
13	Give the surfaces for Verilog module and explain gate instantiations with examples.	Understand	1
	Part – C (Analytical Questions)		
1	Using examples, explain about concurrent and procedural statement with syntaxes.	Understand	2
2	Explain port declaration with an example using Verilog code.	Apply	2
3	Explain the components of a Verilog module with block diagram.	Apply	2
4	Define the following terms relevant to Verilog HDL construct and onventions. (a). Identifiers (b). Strings (c). Data types.	Apply	2
5	Define the following terms relevant to Verilog HDL constructs and conventions. (a). Keywords (b). Strengths (c). Parameters.	Understand	1
6	Explain about number system used in Verilog.	Understand	1
7	Define the following terms relevant to Verilog HDL construct and conventions. (a). Comments, (b). Scalars and vectors. (b). Scalars and vectors.	Understand	1
8	Write about and differences scalars vectors in Verilog module with examples.	Apply	2
9	Define the following terms relevant to Verilog HDL constructs and conventions. (a). Logic values (b). Operators.	Apply	2
10	Write about white space characters and variables with examples.	Apply	2
	UNIT - II **GATE LEVEL MODELING AND MODELING AT DATAFLOW LEVEL**		
	Part – A (Short Answer Questions)		
1	What is gate level modeling?	Understanding	2
2	What is AND gate primitive?	Analyze	2
3	What is module structure? Give the example of module structure.	Analyze	2
4	Define tri-state gate?	Analyze	2
5	What is array of instances of primitives?	Evaluate	2

6	Define delay?	Analyze	2
7	Define strengths and content resolution?	Remember	2
8	What is a net data type?	Remember	2
9	How many types of net data types?	Understand	2
10	How many tri-state gates are there in verilog?	Analyze	2
11	What is continuous assignment structure?	Understand	2
12	What is assignment to vectors?	Understand	2
13	Define operators in verilog?	Understand	2
	Part – B (Long Answer Questions)		
1	Explain in brief built-in primitive gates that are available in Verilog HDL.	Create	2
2	Explain NAND gate primitive with Verilog module.	Evaluate	2
3	Explain NOR gate primitive with Verilog module.	Evaluate	2
4	Design a module for addition of 16 bit words.	Analyze	2
5	What is a three-state gate and explain each type of three-state gate with truth tables?	Evaluate	2
6	Write Verilog HDL source code for a gate level description of 4 to 1 multiplexer circuit. Draw the relevant logic diagram.	Evaluate	2
7	Implement Verilog HDL source code and draw the logic diagram of a 2-to-4 decoder circuit. Give the gate level description.	Understand	2
8	Design module and a test bench for a half-adder.	Evaluate	2
9	Draw the half adder circuits in terms of EX-OR and AND gates. Prepare the half adder module and test bench in terms of and AND gate primitives.	Evaluate	2
10	Design a module and test bench for a full-adder.	Understand	2
11	Design a 4 X 4 multiplier circuit and write its Verilog HDL code.	Understand	2
12	Write a Verilog HDL code for ripple-carry adder using generic specification?	Understand	2
13	Design a 4 bit full adder using gate level primitives and write its HDL code.	Understand	2
	Part – C (Analytical Questions)		
1	Write a Verilog HDL code for n-bit right-to-left shift register using data flow level.	Evaluate	2
2	Give the list of operations in data flow level and give one example for each one. OR Write short notes for the following with examples. a) Unary operators b) Binary operators c) Arithmetic operators d) Logical operators.	Evaluate	2
3	Explain about operator priority with examples.	Evaluate	2
4	Explain bit widths of expressions.	Evaluate	2
5	Design a Verilog module for a 4 to 1 vector multiplexer or module at data flow level.	Evaluate	2
6	Give the block diagram of one digit BCD adder and write its Verilog HDL code. OR Design a Verilog module for a BCD adder module at the data flow level.	Create	2
7	Write a data flow model for a 9-bit parity generator circuit. Use only two assignment statements. Specify rise and fall delays as well.	Apply	2
8	Explain NMOS enhancement with conditions.	Evaluate	2
9	Design a Verilog module of a 4-bit bus switcher at the data flow level.	Evaluate	2
10	Design Verilog module of an edge triggered flip-flop built with the latch at the data flow level.	Evaluate	2

UNIT - III BEHAVIORAL MODELING			
Part – A (Short Answer Questions)			
1	What is behavioral modeling?	Analyze	3
2	What are operations and assignments?	Remember	3
3	Define functional Bifurcation.	Remember	3
4	Define initial construct.	Analyze	3
5	Define always construct.	Analyze	3
6	Explain assignments with delays	Remember	3
7	Define wait construct	Analyze	3
8	Explain multiple always blocks	Analyze	3
9	Define blocking and non-blocking assignments	Evaluate	3
10	Explain the case statement	Analyze	3
11	Draw a simulation flow chart	Analyze	3
12	Explain if and if-else construct	Analyze	3
13	Explain assign and de-assign construct.	Analyze	3
14	Define repeat construct	Evaluate	3
15	Write the syntax for a for loop	Evaluate	3
Part – B (Long Answer Questions)			
1	Write a short note on, (a). Functional bifurcation (b). Intra-assignment delays.	Create	3
2	Write the differences between begin-end and fork-blocks with examples.	Evaluate	3
3	Design up counter coding procedural assignment.	Evaluate	3
4	Write up counter test bench, simulation results.	Analyze	3
5	Write the syntax for the following constructs and give one example for each relevant to behavioral Verilog HDL modeling. (a). initial construct, (b). always construct (c). wait construct.	Evaluate	3
6	What is the difference between an intra- statement delay and an inter-statement delay? explain using an example.	Evaluate	3
7	Write short notes on the following with examples, (a). Intra-assignment delays (b). Delay assignments (c). Zero delay.	Evaluate	3
8	What are the advantages of multiple always blocks? Explain with example.	Remember	3
9	Write a Verilog module for a rudimentary serial transmitter module.	Understand	3
10	Write a model using the behavioral modeling style to describe the behavior of a JK flip- flop using an always statement.	Understand	3
11	(a). Design Verilog module to identify the highest priority interrupts. (b). Write test bench simulation results of above questions with explanation	Analyze	3
12	(a). Design module to convert angels in radians to one in degrees. (b). Write Verilog code above question with explanation.	Remember	3
13	Explain blocking and non-blocking statement with examples.	Evaluate	3
14	Write a Verilog HDL code for n-bit shift register with an enable input using blocking assignments.	Understand	3
Part – C (Analytical Questions)			
1	Write the syntax for the following constructs and give one example for each relevant to behavioral Verilog HDL modeling. (a). assign-deassign construct (b). repeat construct (c). for loop.	Create	3

2	Write the syntax for the following constructs and give one example for each relevant to behavioral Verilog HDL modeling. (a). The disable construct (b). While loop (c). force-release construct.	Evaluate	3
3	Explain about forever loop.	Evaluate	3
4	Define while loop, write syntax with flow chart.	Analyze	3
5	What is the difference between a sequential block and a parallel block? Explain using an example.	Analyze	3
6	(a) Design Verilog code of OR gate using for and disable. (b) Write simulation results of above question with explanation.	Evaluate	3
7	Write syntax for 'for while 'loop and write a Verilog code for n bit Johnson counter.	Evaluate	3
8	Explain event construct in a module.	Evaluate	3
9	Explain stratified event queue.	Evaluate	3
10	Design Verilog module event construct for a serial data receive and test bench for the same.	Evaluate	3
UNIT - 1V SWITCH LEVEL MODELING, SYSTEM TASKS FUNCTIONS AND COMPILER DIRECTIVES			
Part – A (Short Answer Questions)			
1	Explain basic transistor switches.	Analyze	4
2	Define basic switch primitive.	Understand	4
3	Explain the operation of nmos switch.	Understand	4
4	Explain the operation of pmos switch.	Analyze	4
5	Define resistive switches.	Apply	4
6	Define cmos switch.	Remember	4
7	Explain Bi-Directional gates.	Understand	4
8	How to insatiate with strength and delays.	Analyze	4
9	Define system task	Apply	4
10	Define parameter.	Remember	4
11	Explain parameter declaration and assignments.	Understand	4
12	Define module paths.	Analyze	4
13	Define specify block.	Apply	4
14	Define system function.	Remember	4
15	Explain $display Task.	Understand	4
Part – B (Long Answer Questions)			
1	Design half subtractor using CMOS switches.	Understand	4
2	Write the Verilog code for half subtractor using CMOS switches.	Understand	4
3	Design code, test bench, results for CMOS switch with a single control line.	Apply	4
4	Design Verilog module for CMOS flip-flop.	Apply	4
5	Explain bi-directional gates with suitable logic diagrams and give their switch level modeling	Understand	4
6	Design half -adder using CMOS switches.	Understand	4
7	Write the Verilog code for half adder using CMOS switches.	Analyze	4
8	Write about basic switch primitives.	Apply	4
9	Write notes on time delays with switch primitives relevant to switch level modeling.	Understand	4
10	How strength and delays are instantiated? Explain. OR Write notes on instantiations with strength and delays relevant to switch level modeling.	Understand	4

11	Define and explain the following terms relevant to Verilog HDL, (a) Module parameters (b) File-based tasks and functions (c) Compiler directives.	Apply	4
12	Explain parameter declaration and assignments.	Apply	4
13	Explain type declaration for parameters.	Understand	4
14	Explain automatic (recursive) function.	Understand	4
	Part – C (Analytical Questions)		
1	Explain automatic (re-entrant) tasks with example.	Create	4
2	Explain and design Verilog module of timing related parameter with example.	Analyze	4
3	Explain edge sensitive path using an example.	Understand	4
4	Explain overriding parameters.	Apply	4
5	Design Verilog module for left/right shifter.	Apply	4
6	Design Verilog module using path delay.	Apply	4
7	(a) Design Verilog module use of specify block to specify out rise end full time separation for spin delays. (b)Write test bench and simulation for the above.	Analyze	4
8	(a) Design the use of group delay with an ALU module. (b) Write test bench and simulation results for the above.	Evaluate	4
9	What do you mean by User Defined Primitives (UDP) and explain the types with examples	Create	4
10	Give the syntax for function and write a program for 16-to-1 multiplexer using function.	Create	4
	UNIT - V **SEQUENTIONAL CIRCUIT DESCRIPTION, COMPONENT TEST VERIFICATION**		
	Part – A (Short Answer Questions)		
1	What are the types of sequential models?	Understand	5
2	Explain Feedback model.	Analyze	5
3	Explain capacitive model.	Understand	5
4	Explain implicit model.	Understand	5
5	What are the basic memory components?	Understand	5
6	Explain functional register.	Understand	5
7	Define state machine coding.	Analyze	5
8	How do you explain sequential synthesis?	Understand	5
9	What is test bench?	Remember	5
10	How to test a combinational circuit.	Remember	5
11	What is sequential circuit testing?	Understand	5
12	Explain test bench techniques.	Understand	5
13	Define design verification.	Understand	5
14	Define assertion verification.	Understand	5
	Part – B (Long Answer Questions)		
1	What are the various sequential memory storage models? Explain in detail about each of them.	Understand	5
2	Explain cross-coupled NOR latch and all NAND clocked SR latch with the help of neat sketches and write the Verilog cods for each of them.	Understand	5
3	Draw the block diagram of master-slave flip-flop constructed using latches and write the Verilog code for the same.	Analyze	5
4	Explain about sequential UDP with the help of an example.	Apply	5
5	Draw and explain the block diagram of master-slave flip-flop with two feedback blocks using assign statements. Also write the Verilog code for the same.	Understand	5

6	Explain behavioral modeling for D-type latch and the use of non-blocking assignments in latch modeling. Also with the Verilog code for each of them.	Create	5
7	Write and explain the Verilog module for positive edge trigger flip-flop.	Create	5
8	Write a Verilog module for D flip-flop with synchronous control and asynchronous control. And compare the controls of both.	Analyze	5
9	What is function of fork-join construct? Design a Verilog module for D flip-flop using this construct.	Analyze	5
10	Write a Verilog code for D flip-flop using assign and deassign statements.	Understand	5
11	Define setup time. Write a Verilog code for D flip-flop setup time.	Understand	5
12	Define hold time. Design a Verilog module for D flip-flop with hold time.	Understand	5
13	Discuss about setup hold, width and period checks used in Verilog. Write a Verilog module for D flip-flop using setup hold, width and period checks.	Analyze	5
14	Design a Verilog module for the following, i. 8-bit transparent D-Latch ii. 8-bit register with tri-state output.	Apply	5
15	How the memory initialization does is carried out in Verilog? Explain with the help of an example.	Understand	5
	Part – C (Analytical Questions)		
1	Design a Verilog module for 101 moore detector and also obtain its test bench.	Evaluate	5
2.	How the simulation of test bench can be controlled? Explain with help of an example.	Evaluate	5
3	Write a test bench for moore detector for synchronized data input.	Evaluate	5
4	Write a test bench for moore detector to display the synchronization result.	Evaluate	5
5	Write a test bench for moore detector to observe its states.	Evaluate	5
6	Write a Verilog module for 1101 moore detector. Also obtain its test bench and simulation results.	Evaluate	5
7	Write an interactive test bench for 1101 moore detector using display tasks.	Evaluate	5
8	Write a test bench for moore detector to control the delay.	Evaluate	5
9	Write a test bench for moore detector which makes uses of buffer to hold the data.	Evaluate	5
10	Explain in detail about formal verification of a system.	Evaluate	5
11	Write in detail about assertion verification. Also give its benefits.	Evaluate	5
12	What is the function of assert_always monitor? Explain with the help of an example.	Evaluate	5
13	Explain the assert_change and assert_one_hot monitor with the help of an example.	Evaluate	5
14	What is the use of assert_cycle_sequence and assert next? Explain using an example.	Evaluate	5
15	With the help of an example explain about the resetting sequence of controller.	Evaluate	5

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