Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC507

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER-II

B.Tech VIII Semester End Examinations, May - 2020

Regulations: R16

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE

(ECE)

Time: 3 hours **Max. Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1.	a)	Find the output y(n) of a filter whose impulse response is h(n)= {1, 1, 1 } and input signal x(n) = {3, -1, 0,1,3,2,0,1,2,1} overlap save method.	**[7M]**
	b)	Explain about the concept of frequency sampling for developing discrete Time Fourier Transform	**[7M]**
2.	a)	List the major architectural features used in DSP system to achieve high speed program execution?	**[7M]**
	b)	Assuming X(K) as a complex sequence determine the number of complex real multiplies for computing IDFT using direct and Radix-2 FT algorithms?	**[7M]**

UNIT – II

3.	a)	Explain the implementation of 4-bit shift right barrel shifter, with a diagram.	**[7M]**
	b)	Describe the advantages and disadvantages of VLIW architecture	**[7M]**
4.	a)	If a sum of 256 products is to be computed using a pipelined MAC unit, and if the MAC execution time of the unit is 100nsec, what will be the total time required to complete the operation?	**[7M]**
	b)	Explain the assembly instructions memory addressing of VLIW processor with examples	**[7M]**

UNIT – III

5.	a)	Briefly describe the following instructions of TMS320C54XX processors with an example. i) MAC *AR5, +*AR6+, A, B ii) RPT Smem iii) RPTB Pmad iv) BANZ	**[7M]**
	b)	Assume that the current content of AR3 is 400h, what will be its contents after each of the following. Assume that the content of AR0 is 40h.	**[7M]**
6.	a)	Explain the use of DMA Register. Write code to show how the DMA channel 5 context registers can be initialized. Choose arbitrary values to be written in the registers.	**[7M]**
	b)	What will be the contents of accumulator A after the execution of the instruction LD * AR4, 4,A, if the current AR4 points to a memory location whose contents are 8b0eh and the SXM bit of the status register STI is set?	**[7M]**

UNIT – IV

7.	a)	Design an interface to connect a 64K x 16 flash memory to a TMS320C54XX processor. The processor address bus to be used is A0-A15	**[7M]**
	b)	Design a circuit to interface 4K x 16 and a 2K x 16 memory chip to realize program memory space for the TMS320C54xx processor in the address Ranges 03F000h-03FFFFh and 05F800h-05FFFFh, respectively.	**[7M]**
8.	a)	Draw the I/O interface timing diagram for read write read sequence of operation and also explain the signals that are involved in an I/O transaction	**[7M]**
	b)	Explain the use of DMA Register. Write code to show how the DMA channel 5 context registers can be initialized. Choose arbitrary values to be written in the registers	**[7M]**

UNIT – V

9.	a)	Explain about Bit reversed Indexed Generation of TMS320C54XX processor	**[7M]**
	b)	Write a program for Butterfly computation in DIT-FFT Algorithm usingTMS320C54XX Processor	**[7M]**
10.	a)	Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT	**[7M]**
	b)	Explain how the bit reversed index generation can be done in 8 pt FFT. Also write a TMS320C54xx program for 8 pt DIT-FFT bit reversed index generate on.	**[7M]**

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COURSE OBJECTIVES:

The course should enable the students to:

I	Impart the knowledge of basic DSP concepts and number systems to be used, different types of A/D, D/A conversion errors.
II	Learn the architectural differences between DSP and General purpose processor.
III	Learn about interfacing of serial & parallel communication devices to the processor.
IV	Implement the DSP & FFT algorithms.

COURSE OUTCOMES (COs):

CO 1	Understand the basics of Digital Signal Processing and transforms.
CO 2	Able to distinguish between the architectural features of General purpose processors and DSP processors.
CO 3	Understand the architectures of TMS320C54xx devices and Acquire knowledge about various addressing modes of DSP TMS320C54XX.
CO 4	Discuss about various memory and parallel I/O interfaces.
CO 5	Design and implement basic DSP algorithms.

COURSE LEARNING OUTCOMES (CLOs):

AEC507.01	Understand how digital to analog (D/A) and analog to digital (A/D) converters operate on a signal and be able to model these operations mathematically.
AEC507.02	Understand the inter-relationship between DFT and various transforms.
AEC507.03	Understand the IEEE-754 floating point and source of errors in DSP implementations.
AEC507.04	Understand the fast computation of DFT and appreciate the FFT Processing.
AEC507.05	Understand the concept of multiplier and multiplier Accumulator.
AEC507.06	Design SMID ,VLIW architectures.
AEC507.07	Understand the modified bus structures and memory access in PDSPs.
AEC507.08	Understand the special addressing modes in PDSPs.
AEC507.09	Understand the architecture of TMS320C54XX DSPs.
AEC507.10	Understand the addressing modes and memory space of TMS320C54XX DSPs.
AEC507.11	Understand the various interrupts and pipeline operation of TMS320C54XX processors.

AEC507.12	Analyze the Program control, instruction set and programming.
AEC507.13	Understand the concept of on-chip Peripherals.
AEC507.14	Understand the significance of memory space organization.
AEC507.15	Analyze external bus interfacing signals.
AEC507.16	Explain about parallel I/O interface, programmed I/O.
AEC507.17	Understand the significance of Interrupts and Direct Memory Access.
AEC507.18	Understand the basic concepts of convolution and correlation.
AEC507.19	Compare the characteristics of IIR and FIR filters.
AEC507.20	Analyze the concepts of interpolation and decimation filters.

MAPPING OF SEMESTER END EXAMINATION - COURSE OUTCOMES

SEE Question No		Course Learning Outcomes		Course Outcomes	Blooms Taxonomy Level
1	a	AEC507.01	Understand how digital to analog (D/A) and analog to digital (A/D) converters operate on a signal and be able to model these operations mathematically.	CO 1	Remember
	b	AEC507.02	Understand the inter-relationship between DFT and various transforms.	CO 1	Understand
2	a	AEC507.03	Understand the IEEE-754 floating point and source of errors in DSP implementations.	CO 1	Apply
	b	AEC507.04	Understand the fast computation of DFT and appreciate the FFT Processing.	CO 1	Understand
3	a	AEC507.05	Understand the concept of multiplier and multiplier Accumulator.	CO 2	Remember
	b	AEC507.06	Design SMID ,VLIW architectures.	CO 2	Apply
4	a	AEC507.07	Understand the modified bus structures and memory access in PDSPs.	CO 2	Remember
	b	AEC507.08	Understand the special addressing modes in PDSPs.	CO 2	Understand
5	a	AEC507.09	Understand the architecture of TMS320C54XX DSPs.	CO 3	Apply
	b	AEC507.10	Understand the addressing modes and memory space of TMS320C54XX DSPs.	CO 3	Remember
6	a	AEC507.09	Understand the architecture of TMS320C54XX DSPs.	CO 3	Apply
	b	AEC507.10	Understand the addressing modes and memory space of TMS320C54XX DSPs.	CO 3	Remember
7	a	AEC507.16	Explain about parallel I/O interface, programmed I/O.	CO 4	Understand
	b	AEC507.17	Understand the significance of Interrupts and Direct Memory Access.	CO 4	Understand
8	a	AEC507.16	Explain about parallel I/O interface, programmed I/O.	CO 4	Remember
	b	AEC507.17	Understand the significance of Interrupts and Direct Memory Access.	CO 4	Understand
9	a	AEC507.19	Compare the characteristics of IIR and FIR filters.	CO 5	Understand
	b	AEC507.20	Analyze the concepts of interpolation and decimation filters.	CO 5	Remember
10	a	AEC507.19	Compare the characteristics of IIR and FIR filters.	CO 5	Understand
	b	AEC507.20	Analyze the concepts of interpolation and decimation filters.	CO 5	Remember

Signature of Course Coordinator **HOD, ECE**