INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Name	:	HARDWARE AND SOFTWARE CODESIGN
Course Code	:	BES204
Class	:	I - M. Tech
Branch	:	EMBEDDED SYSTEMS
Year	:	2017 – 2018
Course Coordinator	:	Prof. Manisha Guduri, Professor ,ECE
Course Faculty	:	Shashikanth Reddy

OBJECTIVES

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

V. COURSE OBJECTIVES:

At the end of the course, the students will be able to:

i. Analyze and explain the control-flow and data-flow of a software program and a cycle-based hardware description,
ii. Transform simple software programs into cycle-based hardware descriptions with equivalent behavior and vice versa,
iii. Partition simple software programs into hardware and software components, and create appropriate hardware-software interfaces to reflect this partitioning,
iv. Identify performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software components, and
v. Use simulation software to co-simulate software programs with cycle-based hardware descriptions.

VI. COURSE OUTCOMES:

After completing this course the student must demonstrate the knowledge and ability to:

1. Identify and analyze the constraints and characteristics of processor architectures, Hardware, software partitioning distributed system.
2. Understand the typical computer hardware and software components and computer technology trends.
3. Understand the future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure target architectures.
4. Develop the application system and control dominated systems in real time embedded architecture design.
5. Apply the practical consideration in a compiler development environment.
6. Design verification, implementation verification of hardware and software co-designing in the real time applications.
7. Analyze the level specification, design representation for system level synthesis system design-I and design-II.

UNIT-I

CO-DESIGN ISSUES

PART – A (Short Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1.	What is concurrency? Explain its types.	Knowledge	Remember
2.	What are the types of hierarchy? Explain them.	Understand	Understand
3.	What is Meant by FSMD?	Knowledge	Remember
4.	Describe the distributed system co-synthesis	Knowledge	Understand
5.	Explain the concept of Heuristic algorithms?	Understand	Understand
6.	Write your view on hardware/software partitioning?	Knowledge	Remember
7.	Discuss a generic Co-Design methodology?	Knowledge	Understand
8.	What is meant by Reactive system Co-synthesis?	Understand	Remember
9.	Explain system partitioning?	Knowledge	Understand
10.	Explain the conceptual model of specification	Knowledge	Remember

PART – B (Long Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1.	With reference to hardware/software partitioning algorithms explain the following in detail i) Architectural Model ii) Vulcan iii) Controller Architecture	Knowledge	Remember
2.	Explain how the analysis and validation flow will be in a generic co-design methodology?	Understand	Understand
3.	Write short notes on the following. i) Programming constructs ii) Exception handling. iii) Process synchronization	Knowledge	Remember
4.	What is meant by FSMD? Explain an FSMD model for the elevator controller?	Knowledge	Understand
5.	Explain briefly the concepts of i) Finite-state machines ii) Data-Flow Graph. iii) Finite-state machine with data path	Understand	Understand
6.	Explain the following detail with block diagram i) CISC Architecture ii) RISC Architecture	Knowledge	Remember
7.	With reference to the distributed system co-synthesis explain the following i) System partitioning ii) Reactive system co-synthesis	Knowledge	Understand
8.	a) Design hierarchy and explain the different types of hierarchy? i) Structural hierarchy ii) Behavioral hierarchy b) Explain Behavioral Completion	Understand	Remember

UNIT-II

PROTOTYPING AND

PART – A (Short Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1.	What is meant by prototyping?	Knowledge	Remember
2.	Draw the block diagram of Principal structure of an FPGA-based Emulation?	Understand	Understand
3.	Explain operation modes of emulation systems?	Knowledge	Remember
4.	What are steps involved in the FPGA configuration Process?	Knowledge	Understand
5.	Explain Quickturn Emulation Systems?	Understand	Understand
6.	What is meant Aptix prototyping system?	Knowledge	Remember
7.	What are steps in High-Level synthesis?	Knowledge	Understand
8.	Write short notes on target architectures and applications system class?	Understand	Remember
9.	Write short notes on a mixed application that uses 1960 from Intel processor family?	Knowledge	Understand
10.	What is meant by context switching?	Knowledge	Remember

PART – B (Long Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1.	Describe the following with neat sketches. i) Quick turn emulation systems ii) Mentor simExpress emulation system iii) Aptix prototyping system.	Knowledge	Remember
2.	What is meant by prototyping? Discuss the future developments in emulation and prototyping?	Understand	Understand
3.	Clearly Explain the following architecture specialization techniques. i) Component specialization techniques. ii) System specialization techniques.	Knowledge	Remember
4.	With reference to the architectures for control dominated systems explain the following with neat sketches i) 8051-An 8-bit microcontroller architecture. ii) Architectures for high-performance control.	Knowledge	Understand
5.	Construct the block diagram of the ADSP21060 with neat pin diagram with specifications? Discuss in detail about shared memory mapping of the ADSP21060 multiprocessing system	Understand	Understand
6.	Illustrate the role of Prototyping? Evaluate the future developments in emulation and Prototyping of design architecture?	Knowledge	Remember
7.	Construct a neat block diagram of the TMS320C60 data dominated system and discuss in detail with all specifications of the TMS320C60 data dominated system	Knowledge	Understand
8.	What are data-Dominated systems? Explain TMS320C80MVP?	Understand	Remember

UNIT-III

COMPILATION TECHNIQUES

PART – A (Short Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1.	Write design tool requirements of the embedded software development?	Knowledge	Remember
2.	What is mean by source level debugging process?	Understand	Understand
3.	Gives the advantages of the any one of the modern architecture	Knowledge	Remember
4.	Define Interface verification	Knowledge	Understand
5.	Write about design representation for the system level synthesis	Understand	Understand
6.	Define compiler validation strategy?	Knowledge	Remember
7.	Define System simulation based validation strategy	Knowledge	Understand
8.	Difference between compiler validation strategy and System simulation based validation strategy	Understand	Remember
9.	What are the Verification tools of the design verification process?	Knowledge	Understand
10.	Examples of the modern architecture?	Knowledge	Remember

PART - B (Long Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1.	Determined the design representation for the system level synthesis of the Implementation of design application?	Knowledge	Remember
2.	Compare the differences between the following terms of the design verification process, i) Implementation ii) Verification tools iii) Interface verification	Understand	Understand
3.	Describe the problems occurred when adapting traditional compilation model to Embedded Processor?	Knowledge	Remember
4.	Describe the functionality of the Host based compiler validation strategy and System simulation based validation strategy? Write any two differences between them?	Knowledge	Understand
5.	Construct a block diagram of co-simulation model of the design compilation techniques and elaborate the process of the compilation techniques in detail?	Understand	Understand
6.	Estimate the design tool requirements of the embedded software development to develop the embedded processor architecture?	Knowledge	Remember
7.	Elaborate the source level debugging process in the compiler development environment of the embedded architecture	Knowledge	Understand
8.	Are traditional compilation techniques enough to achieve the target in the embedded software development? Justify with your answer correctly?	Knowledge	Remember
9.	Develop the modern architecture of the wireless communication and multimedia with a neat diagram? Gives the advantages of the each modern	Understand	Understand

UNIT-IV

DESIGN SPECIFICATION AND VERIFICATION

PART – A (Short Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1	Define Lycos co-synthesis system?	Knowledge	Remember
2	Write about Co-coordinating concurrent computations?	Understand	Understand
3	Distinguish between shared states versus messages?	Knowledge	Remember
4	Distinguish between open versus closed operations	Knowledge	Understand
5	Define Synthesis Intermediate Forms?	Understand	Understand
6	Define Synthesis Intermediate forms?	Knowledge	Remember
7	Compare between the Blocking operations and Non-blocking operations	Knowledge	Understand
8	Choose the interfacing components of the design specification	Knowledge	Remember
9	What are the tools are present in verification tools?	Understand	Understand

PART – B (Long Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1.	Discuss in detail about design space exploration with Lycos co-synthesis system with neat diagram?	Knowledge	Remember
2.	Define Co-coordinating concurrent computations? Estimate the functionality o coordinating concurrent computations in design specifications?	Understand	Understand
3.	Develop the method of C-VHDL based co-design for Embedded Processor and discuss in detail about the design process with an example?	Knowledge	Remember
4.	Compare between the Blocking operations and Non-blocking operations of the design verification of hardware and software co design?	Knowledge	Understand
5.	Elaborate the process of interfacing components and Programming constructs in design verification?	Knowledge	Remember
6.	Identify the remote procedure calls of the coordinating concurrent computation and discuss in detail of the functionality?	Understand	Understand
7.	Distinguish between the following terms of the coordinating concurrent computations, i) shared states versus messages ii) open versus closed operations	Knowledge	Remember
8.	Define Synthesis Intermediate Forms? Implement the Language-oriented vs Architecture-oriented intermediate forms with neat diagram?	Knowledge	Understand
9.	Define Synthesis Intermediate forms? Describe the process of the synthesis intermediate forms of the design specification and verification in detail?	Understand	Remember
10.	Choose the interfacing components of the design specification and physical realization of the state variables of the design?	Knowledge	Understand

UNIT-V

LANGUAGES FOR SYSTEM

PART – A (Short Answer Questions)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1.	Define multi language co-simulation?	Knowledge	Remember
2.	Difftentaite three factors of the multi language co-simulation model?	Understand	Understand

3.	Define cosyma system?	Knowledge	Remember
4.	Distinguish between cosyma system Lycos system?	Knowledge	Understand
5.	Write about design representation for system level synthesis?	Understand	Remember
6.	Heterogeneous specifications of the system level specifications of the system level design?	Knowledge	Understand
7.	Homogenous specifications of the system level specifications of the system level design?	Knowledge	Remember
8.	Define Lycos system?	Knowledge	Understand
9.	Define multilanguage design flow?	Understand	Remember
10.	hardware and software partitioning of the LYCOS system?	Knowledge	Remember

PART - B (Long Answer Questions)			
S. No	**Questions**	**Blooms Taxonomy Level**	**Course Outcome**
1.	Distinguish between the homogenous and heterogeneous specifications of the system level specifications of the system level design-II?	Knowledge	Understand
2.	Define LYCOS system? Describe the hardware and software partitioning and design space exploration using the LYCOS system?	Understand	Remember
3.	Summarize the hardware and software synthesis using Cosyma system? Illustrate the multi-way partitioning for heterogeneous systems using	Knowledge	Understand
4.	Develop the multilanguage design flow for automotive system with a neat block diagram and examine the design technique levels??	Knowledge	Remember
5.	Difftentaite three factors of the multi language co-simulation model and implementation of the master-slave co-simulation model using require techniques?	Understand	Understand
6.	Define multi language co-simulation and discuss in detail about the multi language co simulation of the design system with an example?	Knowledge	Remember
7.	Develop with a real world example about cosyma system optimization of the design languages system process and discuss the process in detail?	Knowledge	Understand
8.	Develop with a real time example about Lycos system optimization of the design languages system process and discuss the process in detail?	Knowledge	Remember
9.	Illustrate the process of Homogeneous specification and Heterogeneous specifications of the system level design specifications of I and II? Give one example for each specifications?	Understand	Understand
10.	Examine the design technique levels of the Multilanguage design? Gives the different advantages of the system compare to other system level design?	Knowledge	Remember

Prepared by : SHASHIKANTH REDDY, Assistant Professor

Date : 12th SEP 2017.

HOD, ECE