Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC010

INSTITUTE OF AERONAUTICALENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER – II

Four Year B.Tech V Semester End Examinations (Supplementary) - July, 2019

Regulation: IARE-R16

COMPUTER ORGANIZATION

(Electronics and Communication Engineering)

Time:3Hours **Max Marks:70**

Answer any ONE question from each Unit All questions carry equal marks
All parts of the question must be answered in one place only

UNIT – I

1	a)	Briefly explain about general register organization and write about various types of registers. Write about fixed point representation	[7M]
	b)	Calculate the amount of ROM needed to implement a 4bit multiplier.	[7M]
2	a)	Illustrate the connections between the memory and the processor with a neat sketch. Explain the various Instruction types with an example.	[7M]
	b)	An instruction A is stored at location 300 with its adder field at 301. The adder field has value 400. Aprocess register R1contains the number 200. Evaluate the effective address if addressing mode of instruction is i. Direct ii. Immediate	[7M]

UNIT – II

3	a)	Explain in detail about Booth's multiplication algorithm with example.	[7M]
	b)	Calculate the subtraction with the following unsigned decimal numbers by taking the 10's complementofthesubtrahend.123900;090657:100000;000000.	[7M]
4	a)	Describe pipeline. Illustrate four stage instruction pipeline with a neat sketch.	[7M]
	b)	Show the number (+46.5)10 as a floating-point binary number with24bits.	[7M]

UNIT – III

5	a)	Explain the operation of address sequencer in a micro programmed control unit.	[7M]
	b)	Discuss about the design of hardwired control unit with neat diagram.	[7M]

6 a) Illustrate the architecture of pipeline data path. Explain the types of exception in detail with an example. [7M]

b) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome / minimize the sehazards. [7M]

UNIT – IV

7 a) Briefly explain about main memory. What is an auxiliary memory? Write about magnetic disks. [7M]

b) An 8-bit computer has a 16-bit address bus. The first 15 lines of the address are used to select a bank of 32Kbytes of memory. The high-order bit of the address is used to select a register which receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 32K bytes each, for a total of 256K bytes of memory. [7M]

8 a) Explain in detail about the virtual memory and virtual address in address space and memory space. [7M]

b) A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory mapped I/0 configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM,01for ROM,and10 for interface registers. [7M]

i) How many RAM and ROM chips are needed?

ii) Draw a memory-address map for the system.

iii) Give the address range in hexadecimal for RAM, ROM, and interface

UNIT – V

9 a) Explain in detail about DMA driven data transfer technique. [7M]

b) What programming steps are required to check when a source interrupts the computer while it is still being serviced by a previous interrupt request from the same source? [7M]

10 a) Describe the characteristics of super scalar and vector processing. [7M]

b) Explain in detail the various aspects involved in fault tolerance. [7M]

COURSE OBJECTIVES:

The course should enable the students to:

I	Understand the basic structure and operation of a digital computer.
II	Understand the operation of the arithmetic unit including the algorithms &implementation of fixed-point and floating-point addition, subtraction, multiplication & division.
III	Interpret the different types of control and the concept of pipelining.
IV	To study the different ways of communicating with I/O devices and standard I/O interfaces and RISC and CISC processors.
V	To study the hierarchical memory system including cache memories and virtual memory.

COURSE OUTCOMES:

CO 1	Ability to understand the concepts of associated with the computer system design and data representation.
CO 2	Explore the concepts associated with the fixed point arithmetic operations and algorithms.
CO 3	Understand the concepts of Control design of a computer.
CO 4	Ability to learn the concepts associated with the memory organization.
CO 5	Explore the concepts of System Organization including types of interrupts and processors.

COURSE LEARNINGOUTCOMES:

Students who complete the course will have demonstrated the ability to do the following.

AEC010.01	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of acomputer.
AEC010.02	Understand the concepts associated with the computer organization.
AEC010.03	Describe various data representations and explain how arithmetic and logical operations are performed by computers.
AEC010.04	Understand instruction types, addressing modes and theirformats in the assembly language programs.
AEC010.05	Describe the implementation of fixed point and floating point addition, subtraction operations.
AEC010.06	Describe the various major algorithmic techniques (Robertson algorithm, booth‘s algorithm, non-restoring division algorithm).
AEC010.07	Describe the pipeline processing concept with multiple functional units.
AEC010.08	Understand the concept of the modified booth’s algorithm

AEC010.09	Understand the connections among the circuits and the functionalities in the hardwired control unit.
AEC010.10	Describe the design of control unit with address sequencing and microprogramming Concepts.
AEC010.11	Describe the concepts CPU control unit, Pipeline control, instruction pipeline.
AEC010.12	Understand the functionality of super scalar processing and Nano programming.
AEC010.13	Understand the concept of memory hierarchy and different typed of memory chips.
AEC010.14	Describe the concepts of magnetic surface recording, optical memories.
AEC010.15	Understand the cache and virtual memory concept in memory organization.
AEC010.16	Describe the hardware organization of associate memory and understand the read and write operations.
AEC010.17	Understand the various bus control interfaces and system control interfaces.
AEC010.18	Describe the various interrupts (Vectored Interrupts, PCI interrupts, Pipeline interrupts).
AEC010.19	Understand the functionally of RISC and CISC processors.
AEC010.20	Describe the concepts of superscalar and vector processor.

MAPPING OF SEMESTER END EXAMINATION TO COURSE LEARNINGOUTCOMES:

SEE Question No.		Course Learning Outcomes		Course Outcomes	Blooms Taxonomy Level
1	a	AEC010.02	Understand the concepts associated with the computer organization.	CO 1	Understand
	b	AEC010.01	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of a computer.	CO 1	Understand
2	a	AEC010.02	Understand the concepts associated with the computer organization.	CO 1	Understand
	b	AEC010.04	Understand instruction types, addressing modes and their formats in the assembly language programs.	CO 1	Understand
3	a	AEC010.06	Describe the various major algorithmic techniques (Robertson algorithm, booth‘s algorithm, non-restoring division algorithm).	CO 2	Understand
	b	AEC010.05	Describe the implementation of fixed point and floating point addition, subtraction operations.	CO 2	Understand
4	a	AEC010.07	Describe the pipeline processing concept with multiple functional units.	CO 2	Understand
	b	AEC010.05	Describe the implementation of fixed point and floating point addition, subtraction operations.	CO 2	Understand
5	a	AEC010.10	Describe the design of control unit with address sequencing and microprogramming Concepts.	CO 3	Understand
	b	AEC010.09	Understand the connections among the circuits and the functionalities in the hardwired control unit.	CO 3	Understand
	a	AEC010.11	Describe the concepts CPU control unit, Pipeline control, instruction pipeline.	CO 3	Understand

SEE Question No.		Course Learning Outcomes		Course Outcomes	Blooms Taxonomy Level
6	b	AEC010.11	Describe the concepts CPU control unit, Pipeline control, instruction pipeline.	CO 3	Understand
7	a	AEC010.13	Understand the concept of memory hierarchy and different typed of memory chips.	CO 4	Understand
	b	AEC010.13	Understand the concept of memory hierarchy and different typed of memory chips.	CO 4	Understand
8	a	AEC010.15	Understand the cache and virtual memory concept in memory organization.	CO 4	Understand
	b	AEC010.16	Describe the hardware organization of associate memory and understand the read and write operations	CO 4	Understand
9	a	AEC010.17	Understand the various bus control interfaces and system control interfaces.	CO 5	Understand
	b	AEC010.18	Describe the various interrupts (Vectored Interrupts, PCI interrupts, Pipeline interrupts).	CO 5	Understand
10	a	AEC010.20	Describe the concepts of superscalar and vector processor.	CO 5	Understand
	b	AEC010.19	Understand the functionally of RISC and CISC processors.	CO 5	Understand

Signature of Course Coordinator **HOD, ECE**