INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Title	**DIGITAL IC APPLICATIONS USING VHDL**			
Course Code	**AEC516**			
Programme	**B.Tech**			
Semester	**V**			
Course type	**PROFESSIONAL ELECTIVE**			
Regulation	**IARE-R16**			
Course Structure	**Lectures**	**Tutorials**	**Practicals**	**Credits**
	3	**-**	**-**	**3**
Course Coordinator	**Dr. Vijay Vallabhuni, Professor, Department of ECE**			
Course Faculty	**Dr. K Nehru, Professor, Department of ECE** **Mr. D Khalandar Basha, Assistant Professor, Department of ECE**			

I. COURSE OBJECTIVES

The course should enable the students to:

I. Familiarization of Digital Logic families.
II. Design of combinational circuits using digital ICs.
III. Design of sequential circuits using digital ICs.
IV. Strategy of digital circuits using VHDL Programming
V. Acquire knowledge of memories like SRAM, DRAM memories construction, operation and timing diagrams

II. COURSE LEARNING OUTCOMES

Students, who complete the course, will have demonstrated the ability to do the following

S. No	Description
CAEC516.01	Understand logic families of CMOS, TTL and ECL
CAEC516.02	Construct the circuits of CMOS basic gates like inverter, NAND, NOR, AOI and OAI logic with functionality verification.
CAEC516.03	Construct the circuits of TTL logic family by understanding NAND, NOR gates with functionality verification.
CAEC516.04	Identify the need of interfacing CMOS logic family with TTL logic family and interfacing TTL with CMOS logic.
CAEC516.05	Understand the Static and dynamic electrical behavior of CMOS circuits.
CAEC516.06	Understand the different design methods in VHDL.
CAEC516.07	Acquire the basic constucts in VHDL programming.
CAEC516.08	Understand the terms simulation and synthesis in the area of VLSI.
CAEC516.09	Familarization of basic combinational circuits viz decoders, encoders, multiplexers, demultiplexers, parity circuits.
CAEC516.10	Familarization of basic arithmetic circuits for addition, subtraction and multiplication.
CAEC516.11	Distinguish between combinatorial and sequential circuits.
CAEC516.12	Design sequential circuits like latches, flip-flops.
CAEC516.13	Design sequential circuits like shift registers and counters.
CAEC516.14	Understand synchronous design methodology
CAEC516.15	Learns impediments to synchronous design
CAEC516.16	Understand internal structure of SRAM and decoding mechanism
CAEC516.17	Understand timing diagrams of SRAM for read and write operations
CAEC516.18	Understand internal structure of DRAM
CAEC516.19	Understand timing diagrams of DRAM for read and write operations

TUTORIAL QUESTION BANK

S. No	Question	Blooms Taxonomy Level	Course learning Outcome
UNIT-I			
Group – A (Short Answer Questions)			
1	Illustrate negative logic?	Understand	CAEC516.01
2	Define a logic family?	Remember	CAEC516.01
3	Draw the n-channel and p-channel transistors.	Understand	CAEC516.01
4	Draw the CMOS inverter circuit.	Understand	CAEC516.01
5	Classify logic levels for 5V CMOS circuit?	Understand	CAEC516.01
6	How to destroy a CMOS circuit?	Understand	CAEC516.01
7	Define fanout of a circuit?	Remember	CAEC516.01
8	Differntiate enhancement and depletion type of MOSFETs?	Understand	CAEC516.01
9	Define transistion time?	Remember	CAEC516.01
10	Clarify high-impedance state of a circuit?	Understand	CAEC516.01
Group – B (Long Answer Questions)			
1	Explain the operation of n-channel enhancement type MOS transistor and draw characteristic curve .	Understand	CAEC516.02
2	Illustrate the functionality of CMOS NAND gate with a neat sketch and brief the behaviour of the circuit.	Understand	CAEC516.02
3	Illustrate the functionality of CMOS NOR gate with a neat sketch and brief the behaviour of the circuit..	Understand	CAEC516.02
4	Demonstrate the functionality of CMOS XOR gate with a neat sketch and write its truth table.	Remember	CAEC516.02
5	Demonstrate the functionality of CMOS XNOR gate with a neat sketch write its truth table..	Understand	CAEC516.02
6	Explain CMOS circuit steady state electrical behavior and write the limitations for possible charecteristics.	Remember	CAEC516.02
7	ExplainCMOS circuits dynamic electrical behavior along with various cases in each behavior.	Understand	CAEC516.02
8	Draw the TTL NAND gate circuit and justify the behaviour of the circuit as NAND gate.	Understand	CAEC516.02
9	Draw the TTL NAND gate circuit and justify the behaviour of the circuit as NAND gate..	Remember	CAEC516.02
10	Explain about the operation of the emitter coupled logic with a neat sketch and truth table.	Understand	CAEC516.02
Group – C (Problem Solving and Critical Thinking Questions)			
1	Design a CMOS circuit that has the functional behavior $X = \overline{\overline{A}(B + C)}$ and state the functionality verification	Understand	CAEC516.03
2	Implement a CMOS circuit that has the functional behavior $\overline{Y} = AB + \overline{C}$ and justify for the functionality described.	Remember	CAEC516.03
3	Design a CMOS circuit that has the functional behavior $\overline{Z} = AB + C\overline{D}$ and verify the functionality	Understand	CAEC516.03
4	Build the CMOS AND gate in transistor level and expain different tropologies for drwing the schematic.	Remember	CAEC516.03
5	Explain why the number of CMOS inputs connected to the output of a CMOS gate generally is not limited by DC fanout considerations with example.	Understand	CAEC516.03
6	Draw and explin CMOS circuit for or-and-invert logic for the boolean expression Y = (AB + CD)'.	Remember	CAEC516.04
7	Construct a CMOS circuit for and-or-invert gate to functionate for the boolean expression Y = ((A+B)(C+D))' .	Remember	CAEC516.04
8	Draw a circuit diagram, function table, and logic symbol in the style of CMOS 2 input AND gate with two inputs A and B and an output Z,	Remember	CAEC516.05

S. No	Question	Blooms Taxonomy Level	Course learning Outcome
	where Z=1 if A=0 and B=1, and Z=0 otherwise.		
9	Present a circuit diagram, function table, and logic symbol in the style of CMOS 2 input AND gate with two inputs A and B and an output Z, where Z=0 if A=1 and B=0, and Z=1 otherwise.	Understand	CAEC516.05
10	Explain the need of CMOS- TTL interfacing and how to interface CMOS with TTL gate.	Remember	CAEC516.05
UNIT-II			
Group – A (Short Answer Questions)			
1	What is the acronym of VHDL?	Understand	CAEC516.06
2	Define synthesis?	Understand	CAEC516.06
3	Describe the role of Place and route?	Understand	CAEC516.06
4	Review entity in VHDL programming?	Understand	CAEC516.06
5	What is timing verification?	Understand	CAEC516.06
6	Discuss about the role of compilation?	Remember	CAEC516.06
7	Write the syntax of architecture?	Understand	CAEC516.06
8	How to declare a signal and write its syntax.	Remember	CAEC516.06
9	Delare a component in VHDL programming with an example.	Understand	CAEC516.06
10	Differentiate signal and wire in VHDL programming?	Understand	CAEC516.06
Group – B (Long Answer Questions)			
1	Expand the term VHDL and list the features of VHDL. ?	Remember	CAEC516.06
2	Draw and explain the design flow of VHDL and breif in detail about each block?	Understand	CAEC516.06
3	Explain the program structure of VHDL. Explain the significance of entity and architecture.	Understand	CAEC516.06
4	Differentiate types and constants in VHDL programming explain each with an example.	Remember	CAEC516.06
5	Summarize libraries and packages in VHDL programming. What is the need of them.	Understand	CAEC516.06
6	Write short note on the structural design style of VHDL programming with suitable example.	Understand	CAEC516.06
7	Explain the behavioural design style of VHDL programming with suitable example.	Understand	CAEC516.06
8	Describe the dataflow design style of VHDL programming with suitable example.	Understand	CAEC516.06
9	What is a mixed design style of VHDL programming with suitable example.	Remember	CAEC516.06
10	Compare the various programming styles of VHDL language with respect to their signifance.	Understand	CAEC516.06
Group – C (Problem Solving and Critical Thinking Questions)			
1	Describe the following with a suitable example. i. std_logic ii. std_logic_vector iii. Constant.	Understand	CAEC516.07
2	Explain transport and inertial delay model in VHDL using an inverter with a delay of 20 nsecs. Develop a VHDL code for above two models. Assume delay of wire = 10 nsecs.	Understand	CAEC516.07
3	List the three styles of modeling a digital system in VHDL. Give the VHDL code for each of them, with reference to half adder.	Remember	CAEC516.07
4	List the seven classes of VHDL operators according to their precedence and indicate the order of evaluation of the expression, A & not B or C nor D.	Understand	CAEC516.07
5	Explain the following giving requisite statements of VHDL: i) Transport delay ii) Inertial delay.	Understand	CAEC516.07
6	What are VHDL functions? Where do they appear? Give the complete VHDL code to find 2's complement of a N-bit number.	Remember	CAEC516.07

S. No	Question	Blooms Taxonomy Level	Course learning Outcome
7	Write a VHDL code to model the Boolean expression, $F(A,B,C) = \sum m(0,3,5,6,7)$. Using process statement.	Understand	CAEC516.07
8	Discuss various datatypes in VHDL with examples.	Understand	CAEC516.07
9	What is meant by variables, signals and constants in VHDL? Compare signals with variables, give an example for each.	Remember	CAEC516.07
10	Write a VHDL code for a full subtractor using logic equation.	Remember	CAEC516.07
UNIT-III			
Group – A (Short Answer Questions)			
1	Define a binary decoder?	Remember	CAEC516.08
2	Draw the logic symbol of 74x138.	Understand	CAEC516.08
3	Draw the 2 to 4 decoder logic circuit.	Understand	CAEC516.08
4	What is priority encoder?	Remember	CAEC516.08
5	What is three state buffer?	Remember	CAEC516.08
6	What is magnitude comparator?	Understand	CAEC516.08
7	Draw the full adder circuit truth table.	Understand	CAEC516.09
8	What are the applications of code converters?	Remember	CAEC516.09
9	What is carry look ahead adder?	Remember	CAEC516.09
10	What is ripple carry adder?	Remember	CAEC516.09
11	Write merits and demerits of carry look ahead adder.	Understand	CAEC516.09
12	Specify the need of parity generators and parity checkers.	Understand	CAEC516.09
13	Represent the functionality of full subtractor in the form of truth table.	Remember	CAEC516.09
14	Draw the full adder circuit using half adder.	Understand	CAEC516.09
Group – B (Long Answer Questions)			
1	Explain the functionality of 3 to 8 decoder IC and draw it gate level structure.	Understand	CAEC516.10
2	Expalin about 74x148 IC with the help of its truth table and specify its significance.	Understand	CAEC516.10
3	Contrast 4x1 multiplexers and 1x4 demultiplexors behaviour and specify it application.	Remember	CAEC516.10
4	Explian about iterative compartor circuit. Design a 16 bit comparator using iterative concept	Understand	CAEC516.10
5	Design the gate level half adder circuit with suitable gates and write its truth table.	Understand	CAEC516.10
6	Realize the full adder circuit using half adder and explain the functionality with truthtable.	Remember	CAEC516.10
7	Draw and explain 4-bit ripple carry adder. Write the advantages of ripple carry adder?	Understand	CAEC516.10
8	Realize the binary to BCD code conversion with truth table and extract the boolean expressions for conversion.	Understand	CAEC516.10
9	Explain the working principle of combinational multiplier circuits with suitable diagram.	Remember	CAEC516.10
10	Draw and explain about carry look ahead adder. Explain the need of carry look aheader?	Remember	CAEC516.10
11	Implement structural model for 4- bit carry look ahead adder and draw the Boolean expressions for carry generation and carry propagation	Understand	CAEC516.10
12	Model a structural model for 4- bit ripple carry adder and draw the Boolean expressions for sum and carry in each block	Understand	CAEC516.10
Group – C (Problem Solving and Critical Thinking Questions)			
1	Write VHDL models for a 4-to-1 multiplexer with its respective design construct element.	Remember	CAEC516.10
2	Design a binary multiplier and hence write VHDL code for 4x4 multiplier using behavioural model.	Understand	CAEC516.10

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3	With the help of case construct, write VHDL code for 8 to 3 priority encoder	Understand	CAEC516.10
4	Write the VHDL code using structural description for the 4-bit adder as a ripple carry adder.	Remember	CAEC516.10
5	Develop a VHDL structural model for the 4x1 multiplexer, using three state logic.	Understand	CAEC516.10
6	Mention VHDL code for a parity generator. Use component declaration for the program.	Understand	CAEC516.10
7	Write a VHDL program to model a 4 bit comparator and explain the same briefly.	Understand	CAEC516.11
8	Realize 8:1 multiplexer using 2:1 multiplexer and model its VHDL model in suitable design style	Understand	CAEC516.10
8	Model 8:3 encoder using VHDL behavior constrcts and explain the functionality of the same briefly.	Understand	CAEC516.11
9	Give a VHDL code to implement a 2:4 decoder with an active low enable line using, i) conditional signal assignment. ii) Selected signal assignment statement. Use '&' operator as required.	Understand	CAEC516.11
10	Model a 3-8 decoder with enable input using VHDL use any one of the allowed design methods.	Understand	CAEC516.11
11	Design 3 to 8 decoder using 2 to 4 decoder and implement its VHDL model along with circuit.	Understand	CAEC516.10
12	Implement 16x1 multiplexer behavioural model in VHDL using if construct.	Understand	CAEC516.10
UNIT-IV			
Group – A (Short Answer Questions)			
1	Outline about barrel shifter.	Remember	CAEC516.12
2	Illusrate is floating point encoder.	Remember	CAEC516.12
3	Explain about dual-priority encoder.	Remember	CAEC516.12
4	What is a latch?	Understand	CAEC516.12
5	What is a flip flop?	Understand	CAEC516.12
6	Summarize various types of shift registers	Understand	CAEC516.12
7	Differentiate synchrounous and asynchronous counter.	Understand	CAEC516.12
8	Contrast the primary difference between synchoronous and asynchronous circuits.	Understand	CAEC516.12
9	Define PROM.	Understand	CAEC516.12
10	What is the difference between PLA and PAL?	Understand	CAEC516.12
Group – B (Long Answer Questions)			
1	Differentiate the imortant characteristics of the latch and flip flops used in the memory circuits?	Understand	CAEC516.13
2	Explain about various types of operations performed in shift register for the shifting of bits.	Understand	CAEC516.13
3	Realize T flip flop using minimum number of JK flip flops by satisfying T flip flop excitation table.	Understand	CAEC516.13
4	Draw and explain about MOD-6 counter with relevant diagrams and desccription.	Understand	CAEC516.13
5	Draw and explain about synchronous counters with neat block diagrams and table.	Understand	CAEC516.13
6	Write short note on synchronous design methodology used in the digital circuits.	Understand	CAEC516.13
7	Draw and explain about programmable read only memory with necessry block diagrams.	Understand	CAEC516.13
8	Expalin various types of ROMs used in the storing of data in the combinational circuits.	Understand	CAEC516.13

S. No	Question	Blooms Taxonomy Level	Course learning Outcome
9	Write short note on impediments to synchronous design for the digital design applicaitons.	Understand	CAEC516.13
10	What are the differences between PLA, PAL and PROM in reference to their characeritsitcs?	Understand	CAEC516.13
Group – C (Problem Solving and Critical Thinking Questions)			
1	Write VHDL description for mod-14 up-down counter with required figures and tables.	Understand	CAEC516.14
2	Give a VHDL code to model D-Flip flop, assuming D, clock, preset and clear as the inputs and Q, Qbar as the output. Use process statement.	Understand	CAEC516.14
3	Present a behavioural code for a 4-bit shift register using D-flip flops with neat block diagrams.	Understand	CAEC516.14
4	Develop a VHDL code to model an 4-bit synchronous counter using D flip flops. Write its VHDL model.	Understand	CAEC516.14
5	Using VHDL process, model the JK flip flop having set and reset pins with neat sketches.	Understand	CAEC516.14
6	Write a VHDL code for a 4 bit ripple counter, built using D flip-flops. Also mention its block diagram and functional tables.	Understand	CAEC516.14
7	Give the VHDL code that models 4-bit up-down synchronous counter with required plots.	Understand	CAEC516.15
8	Using the VHDL code of state machine, write the logic to detect the sequence “1001” on a data input then produce a logic ‘1’ output when the sequence has been detected.	Understand	CAEC516.15
9	Write a VHDL code for 3-bit ripple up counter employing JK flip-flops using structural style of modeling.	Understand	CAEC516.15
10	Develop a VHDL code for positive edge triggered D flip flop with active high reset asynchronous input using guarded block statement.	Understand	CAEC516.15
UNIT-V			
Group – A (Short Answer Questions)			
1	What are the advantages of FPGA?	Understand	CAEC516.16
2	What is the Difference between RAM and ROM?	Remember	CAEC516.16
3	What is the Difference between SRAM and DRAM?	Remember	CAEC516.16
4	What are the advantages of EEPROM?	Remember	CAEC516.16
5	Draw the block diagram of memory cell.	Understand	CAEC516.16
6	Draw 6T SRAM cell.	Remember	CAEC516.16
7	What is the advantage of address multiplexing.	Remember	CAEC516.16
8	How to remove the data stored in EEPROM.	Remember	CAEC516.16
9	Draw 1-bit DRAM cell.	Remember	CAEC516.16
10	Define latency in memory cells.	Understand	CAEC516.16
Group – B (Long Answer Questions)			
1	Draw and explain about block diagram of RAM cell with the necessary plots and tables.	Understand	CAEC516.17
2	Give the read and write operation of RAM w.r.t timing waveform and block diagrams.	Understand	CAEC516.17
3	Elaborate the schematic of DRAM and explain the operation with timing diagrams.	Understand	CAEC516.17
4	Draw and explain about 4x4 ROM with neat figures and functional tabluar forms.	Understand	CAEC516.17
5	Explain about 2D decoding methodology used in the memory circuits for digital applications.	Understand	CAEC516.17
6	Draw and explain about read and write operations of DRAM with neat block diagrams.	Understand	CAEC516.17
7	Discuss about SRAM operation in reference its block diagrams and mention the advantages.	Understand	CAEC516.18
8	Mention tge synchronous SRAM with corresponding figures and timing waveforms.	Understand	CAEC516.18

S. No	Question	Blooms Taxonomy Level	Course learning Outcome
9	Differentiate salient features of SRAM and DRAM in reference to their working principle.	Understand	CAEC516.18
10	Explain about synchronous DRAM with neat timing waveforms and block diagrams.	Understand	CAEC516.18
Group – C (Problem Solving and Critical Thinking Questions)			
1	Explain static RAM memory. Write simple memory model in VHDL using dataflow style.	Understand	CAEC516.19
2	State the difference between PROM and PLA. Implement full adder using PROM.	Understand	CAEC516.19
3	What is a programmable logic device? Explain EPROM and EEPROM cells used to establish the programmable connection.	Understand	CAEC516.19
4	Discuss general model of melay sequential machine. How do you realize mealy sequential network with ROM?	Understand	CAEC516.19
5	Write the behavioral description to simulate 8 byte RAM with Read/write line, address data lines, and active low chip select line. Implent the read and write operations in the architecture.	Understand	CAEC516.19
6	Write a block diagram and function table of 128x16 static memory and explain its working priniple.	Understand	CAEC516.19
7	Write the block diagram and function table of a SRAM cell and explain its working style.	Understand	CAEC516.19
8	Design a 256x8 ROM that converts from 8-bit binary to 8-bit gray code and give its convertion table.	Understand	CAEC516.19
9	Design a ROM block to function as a full adder and present the corresponding block diagrams.	Understand	CAEC516.19
10	Draw a logic symbol for and determine the size of a ROM that reliazes an JK flip flop.	Understand	CAEC516.19

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