INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500043

INFORMATION TECHNOLOGY

TUTORIAL QUESTIONBANK

Course Name	**:**	**DIGITAL LOGIC DESISN**
Course Code	**:**	**AEC020**
Class	**:**	**B Tech III Semester**
Branch	**:**	**CSE**
Academic Year	**:**	**2018– 2019**
Course Coordinator	**:**	**Mr. K.Ravi, Assistant Professor, ECE**
Course Faculty	**:**	**Ms. G.Bhavana, Assistant Professor, ECE**

COURSE OBJECTIVES:

The course should enable the students to:

S.No	Description
I	Familiarize the basic concept of number systems, Boolean algebra principles and minimization techniques for Boolean algebra.
II	Analyze Combination logic circuit and sequential logic circuits such as multiplexers, adders, decoders flip-flops and latches
III	Understand about synchronous and asynchronous sequential logic circuits.
IV	Impart the basic understanding of memory organization, ROM, RAM, PLA and PAL.

COURSE LEARNING OUTCOMES:

Students, who complete the course, will have demonstrated the ability to do the following:

AEC020.01	Understand the basic concept of number systems, binary addition and subtraction for digital systems.
AEC020.02	Explain 2's complement representation and implement binary subtraction using 1's and 2's complements.
AEC020.03	Discuss about digital logic gates, error detecting and correcting codes for digital systems.
AEC020.04	Describe the importance of SOP and POS canonical forms with examples.
AEC020.05	Describe minimization techniques and other optimization techniques for Boolean formulas in general and digital circuits.
AEC020.06	Evaluate Boolean algebra expressions by minimizing algorithms like sop and pos using Boolean Postulates and theorems.
AEC020.07	Solve various Boolean algebraic functions using Karnaugh map and Tabulation Method.
AEC020.08	Understand bi-stable elements and different type's combinational logic circuits.
AEC020.09	Analyze the design procedures of Sequential logic circuits with the help of registers
AEC020.10	Discuss the concept of flip flops and latches by using sequential logic circuits.
AEC020.11	Differentiate combinational logic circuits with sequential logic circuits along with examples.
AEC020.12	Understand the concept of memory organization, read only memory and random access memory.

AEC020.13	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.
AEC020.14	Explain the concept of memory hierarchy in terms of capacity and access time.
AEC020.15	Explain about Synchronous and Asynchronous Sequential Circuits: Reduction of state tables for Mealy and Moore machines
AEC020.16	Discuss about various memory concepts with respect to temporary and permanent memory organizations.

TUTORIAL QUESTION BANK

S. No	Question	Blooms Taxonomy Level	Course learning Outcome
	UNIT I NUMBERS SYSTEMS AND CODES		
	PART-A(Short Answer Questions)		
1.	Write short notes on binary number systems?	Understand	CAEC020.1
2.	Discuss 1"s and 2"s complement methods of subtraction?	Understand	CAEC020.1
3.	Discuss octal number system?	Understand	CAEC020.1
4.	Discuss about BCD code?	Understand	CAEC020.1
5.	Solve If $(2.3)_6+(1.2)_2=(y)_4$ then find y?	Understand	CAEC020.1
6.	Write a short note on four bit BCD codes?	Understand	CAEC020.1
7.	Explain the specialty of unit –distance code? State where they are used?	Understand	CAEC020.1
8.	Write a short note on error correcting codes?	Understand	CAEC020.1
9.	Solve $(127)_8$ to all number systems?	Understand	CAEC020.1
10.	Discuss what a logic design is and what do u mean by positive logic system?	Understand	CAEC020.1
11.	Convert $(4085)_8$ into base-5?	Understand	CAEC020.1
12.	Convert $(4085)_8$ into base-3?	Understand	CAEC020.1
13.	Write the steps involved in unsigned binary subtraction using complements with examples?	Understand	CAEC020.1
14.	Explain the addition of two signed binary number along with examples?	Understand	CAEC020.1
15.	Differentiate between binary code and BCD code?	Understand	CAEC020.1
16.	Solve subtraction between 9-5 using xs-3?	Understand	CAEC020.1
17.	Convert (4085)9 into base-4?	Understand	CAEC020.1
18.	Convert 10101101.0111 to octal equivalent and hexadecimal equivalent?	Understand	CAEC020.1
19.	Convert the octal numbers into binary, decimal and Hexadecimal numbers (45.5)octal,(32.2)octal?	Understand	CAEC020.1
20.	Convert the following Hexadecimal numbers to their De equivalent EAF1?	Understand	CAEC020.1
	PART-B(Long Answer Questions)		
1.	(a) Solve the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend: i.100–110000 ii. 11010 -1101. (b) Construct a table for 8 4 2 1 weighted code and write 2421 using this code .Write short notes on binary number systems.	Understand	CAEC020.1
2.	(a) Solve arithmetic operation indicated below. Follow signed bit notation: i. 001110+110010 ii. 101011 - 100110.	Understand	CAEC020.1

	(b) Explain the importance of gray code?		
3.	Solve $(3250 - 72532)_{10}$ using 10's complement?	Understand	CAEC020.1
4.	Explain about self-complemented codes?	Understand	CAEC020.1
5.	Solve (a) Divide 01100100 by 00011001, (b) Given that $(292)_{10} = (1204)_b$ determine `b'	Understand	CAEC020.1
6.	Differentiate between BCD code and 2421 code and XS-3 code?	Understand	CAEC020.1
7.	Solve the following, a) Find (72532 - 03250) using 9's complement. b) Show the weights of three different 4 bit self-complementing codes whose only negative weight is - 4 and write down number system from 0 to 9.	Understand	CAEC020.1
8.	Solve $(3250 - 72532)_{10}$ using 9's complement with XS-3?	Understand	CAEC020.1
9.	State 89+54 using XS-3?	Understand	CAEC020.1
10.	Solve the following numbers, (a) Add 01100100 by 00011001 (b) Given that $(542)_6 = (b)_4$ determine `b'	Understand	CAEC020.1
11.	Solve, (a) What is the gray code equivalent of the Hex Number3A7 (b) Find 9's complement $(25.639)_{10}$	Understand	CAEC020.1
12.	Apply the representation of +65 and -65 in sign magnitude Sign 1"s complement and sign 2"s complement representation?	Understand	CAEC020.1
13.	State different ways for representing the signed binary numbers?	Understand	CAEC020.1
14.	Solve addition and subtraction of $(456)_2$ and $(341)_2$using BCD and XS-3?	Understand	CAEC020.1
15.	Define weighted codes and non weighted codes with examples?	Remember	CAEC020.1
16.	Explain what do you mean by error detecting and correcting codes?	Understand	CAEC020.1
17.	Illustrate the rules for XS3 addition and subtraction?	Understand	CAEC020.1
18.	Explain error occurred in the data transmission can be detected using parity bit?	Understand	CAEC020.1
19.	Solve addition between 95 and 62 using BCD and XS-3Method?	Understand	CAEC020.1
20.	Solve subtraction 67 and 73 using BCD and Xs-3 Method?	Understand	CAEC020.1
PART-C(Problem Solving Critical Thinking Questions)			
1.	Solve Subtraction and Addition 617 and 732 using BCD andXs-3 Method?	Understand	CAEC020.1
2.	Convert the octal numbers into binary, decimal, BCD and Hexadecimal numbers $(36.6)_8$,$(45.5)_8$,$(26.3)_8$,$(48)_8$.	Understand	CAEC020.1
3.	Solve Subtraction and Addition 4327 and 1562 using BCD andXs-3 Method?	Understand	CAEC020.1
4.	Find transmitted 11 bits for 0110001 when hamming code is used?	Understand	CAEC020.1
5.	Explain in brief about weighted and non weighted codes?	Remember	CAEC020.1
6.	write the octal representation of the following fractional numbers:(0.5)d,(1.5)d,(2.333)d,(3.875)d,(13.125)d,(14.666)d.	Understand	CAEC020.1
7.	Find the illegal representation in the following: (120A)d,(1010011)BCD, (0208)octal, (10102011)b, (GC0A)h.	Understand	CAEC020.1
8.	Convert the binary number to hexadecimal number: i. 0100001011010011,010110101001111 ii. 01111111.1100011	Understand	CAEC020.1

9.	Convert the hexadecimal number to binary number: 0x5A9F, 42D3.	Understand	CAEC020.1
10.	Understand by two examples that two's compliment of a number taken twice returns the original number?	Understand	CAEC020.1
UNIT II BOOLEAN ALGEBRA AND GATE LEVEL MINIMIZATION			
PART-A(Short Answer Questions)			
1.	Define K-map? Name its advantages and disadvantages?	Remember	CAEC020.6
2.	Define Implicant, prime Implicant and Essential prime Implicant?	Remember	CAEC020.2
3.	Define Consensus Theorem?	Remember	CAEC020.2
4.	Describe types of minimization techniques?	Remember	CAEC020.6
5.	Summarize the Boolean function x′yz + x′yz′ + xy′z′ + xy′z using K-map?	Remember	CAEC020.2
6.	Explain three variable k-map with example?	Remember	CAEC020.6
7.	Solve AB^{I}+BC+CA=AB+BC	Remember	CAEC020.2
8.	Design the two graphic symbols for NAND gate?	Remember	CAEC020.2
9.	Design the two graphic symbols for NOR gate?	Remember	CAEC020.2
10.	Summarize the Boolean function x′yz + x′yz′ + xy′z′ + xy′z without using K- map?	Remember	CAEC020.6
11.	Explain the properties of EX-OR gate?	Remember	CAEC020.2
12.	Solve any three bit function and implement it with AND-OR INVRET gates?	Remember	CAEC020.2
13.	Solve the following Boolean function using K-map a) ABC^{I} + A^{I}BC +AB	Remember	CAEC020.6
14.	Solve the following using NAND gates? a) (A+B)(C+D) b) A.B+CD(AB^{I}+CD)	Remember	CAEC020.6
15.	Sketch the following equation using k-map and realize it using NAND gate? Y=∑m(4,5,8,9,11,12,13,15)	Remember	CAEC020.6
16	Solve Y=AB^{I}+CD+(A^{I}B+$C^{I}D^{I}$) using NAND gate?	Remember	CAEC020.2
17	State that AND-OR network is equivalent to NAND-NAND network?	Remember	CAEC020.2
18	Show both NAND and NOR gates are called Universal gates?	Remember	CAEC020.2
19	Sketch the following logic function using k-map and implement it using logic gates? Y(A,B,C,D)= ∑m(0,1,2,3,4,7,8,9,10,11,12,14)	Remember	CAEC020.2
20	Summarize the rules and limitations of K-map simplification?	Remember	CAEC020.6
21	Analyze the steps for simplification of POS expression?	Remember	CAEC020.6
PART-B(Long Answer Questions)			
1.	A combinational circuit has 4 inputs(A,B,C,D) and three outputs(X,Y,Z)XYZ represents a binary number whose value equals the number of 1's at the input (i) state the min term expansion for the X,Y,Z (ii). state the max term expansion for the Y and Z	Remember	CAEC020.6
2.	Minimize the following function using K-map. F (A, B, C, D) = ∑m (1,3,5,7,9,10,11,12,15)	Remember	CAEC020.6
3.	Minimize the following function using K-map f =∑m(1,2,3,5,12,13,15)	Remember	CAEC020.6
4.	Design BCD to Gray code converter and realize using logic gates?	Remember	CAEC020.2
5.	Design all logic gates using NAND gate?	Remember	CAEC020.2

6.	compile the following expression using Karnaugh map ($B^{II}A + A^{II}B + AB^{II}$)	Remember	CAEC020.2
7.	Design a circuit with three inputs (A, B, C) and two outputs(X, Y) where the outputs are the binary count of the number of‘ON"(HIGH) inputs?	Remember	CAEC020.6
8.	Implement the INVERTER gate, OR gate and AND gate using NAND gate, NOR gate?	Remember	CAEC020.2
9.	Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7?	Remember	CAEC020.2
10.	Implement Half adder using 4 NAND gates?	Remember	CAEC020.2
11.	Implement the Boolean function F = AB + CD + E using NAND gates only?	Remember	CAEC020.6
12.	Summarize the Boolean function $F(w, x, y, z) = \Sigma(1, 3, 7, 11,15) + \Sigma d(0. 2, 5)$	Remember	CAEC020.6
13.	Implement following expression f= a+b+c in to canonical SOP and convert it to pos using k-map?	Remember	CAEC020.6
14.	Implement following expression f= abc in to canonical POS and convert it to SOP using k-map?	Remember	CAEC020.6
15.	Identify all the prime implicants and essential prime implicants of the following functions using k- map $F = \Sigma m (0, 1, 2, 3, 4,10, 11, 14, 15)$	Remember	CAEC020.6
16.	Identify all the prime implicants and essential prime implicants of the following functions Using k- map. $F(A,B,C,D) = \Sigma m(0,1,2,5,6,7,8,9,10,13,14,15)$.	Remember	CAEC020.6
17.	Identify all the prime implicants and essential prime implicants of the following functions Using k- map. $F(A,B,C) = \Sigma m(0,1,2,6,7).+\sum d(3,5)$	Remember	CAEC020.6
18.	Design alternate symbols for all the gates?	Remember	CAEC020.2
19.	Design all the logic gates using NOR gate?	Remember	CAEC020.2
20.	Identify all the prime implicants and essential prime implicants of the following functions Using k- map. $F(A,B,C,D) = \pi M(0,1,2,5,6,7,8,9,10,13,14,15)$.	Remember	CAEC020.6
PART-C(Problem Solving Critical Thinking Questions)			
1.	Use De-Morgan theorem to simplify $F=(A+B+C.D.E)^1$.	Remember	CAEC020.2
2.	State that for constructing XOR from NANDs we need four NAND gates?	Remember	CAEC020.2
3.	Convert A.B.C+A.D expression into standard SOP format?	Remember	CAEC020.2
4.	Convert (A+B+C).(A+D) expression into standard POS format?	Remember	CAEC020.2
5.	Construct XOR and XNOR from NAND and NOR gates?	Remember	CAEC020.2
6.	Construct SOP expression and POS expression for a four input NAND gate?	Remember	CAEC020.2
7.	Understand and explain five variable k-maps with an example?	Remember	CAEC020.6
8.	Find the logic function $F=(AB+BC+E)^1$ using AND-OR two level realization?	Remember	CAEC020.6
9.	Design a 5-variable k-map. $F(A,B,C,D,E)=\pi M(0,1,2,5,6,7,8,9,10,13,14,15,17,19,20).\pi d(3,25,28,30,31)$	Remember	CAEC020.6
10	Design a 5-variable k-map. $F(A,B,C,D,E)=\sum m(0,1,2,5,6,7,8,9,10,17,19,20)+\sum d(3,12,15,18,25,28,30,31)$	Remember	CAEC020.6
UNIT-III DESIGN OF COMBINATIONAL CIRCUITS			
PART-A(Short Answer Questions- CIE- I)			

1.	Explain the design procedure for combinational circuits?	Understand	CAEC020.8
2.	Apply various code conversion methods?	Understand	CAEC020.8
3.	Design a 4-bit binary to BCD converter?	Understand	CAEC020.8
4.	Design and implement an 8421 Gray code converter?	Understand	CAEC020.8
5.	Design a combinational logic circuit with 3 input variables that will produce logic 1 output when more than one input variables are logic 1?	Understand	CAEC020.8
6.	Compose and explain the block diagram of 4-bit parallel adder?	Understand	CAEC020.8
7.	Design a logic circuit to convert BCD and gray code?	Understand	CAEC020.8
8.	Design a full adder using two half adders?	Understand	CAEC020.8
9.	Explain magnitude comparator? Design a 1-bit comparator using logic gates?	Understand	CAEC020.8
10.	Compose the circuit for 3 to 8 decoder and explain it with logic gate?	Understand	CAEC020.8
PART-A(1) (Short Answer Questions-CIE- II)			
11.	Construct the logic circuit for full subtractor using decoder?	Understand	CAEC020.8
12.	Define binary decoder? Explain the working of 2:4 binary decoder?	Understand	CAEC020.8
13.	Design Full adder using a suitable Decoder?	Understand	CAEC020.8
14.	Define encoder? Design octal to binary encoder?	Understand	CAEC020.8
15.	Design a 4-bit priority encoder?	Understand	CAEC020.8
16.	Design the block diagram of a 4:1 multiplexer using 2:1multiplexer?	Understand	CAEC020.8
17.	Define Multiplexer and demultiplexer?	Understand	CAEC020.8
18.	Explain how decoder acts as a demultiplexer?	Understand	CAEC020.8
19.	Differentiate multiplexer and demultiplexer?	Understand	CAEC020.8
20.	Explain the working of 8:1 multiplexer?	Understand	CAEC020.8
PART-B(Long Answer Questions-CIE-I)			
1.	Design a combinational circuit that generates logic „1“ for odd inputs?	Understand	CAEC020.8
2.	Design a logic circuit to convert gray code to binary code?	Understand	CAEC020.8
3.	Design circuit to detect invalid BCD number and implement using NAND gate only?	Understand	CAEC020.8
4.	Explain the design procedure for code converter with the help of example?	Understand	CAEC020.8
5.	Construct half subtractor using NAND gates?	Understand	CAEC020.8
6.	Explain the working of carry look-ahead generator?	Understand	CAEC020.8
7.	Explain carry propagation in parallel adder with neat diagram?	Remember	CAEC020.8
8.	Explain the circuit diagram of full subtractor and full adder?	Understand	CAEC020.8
9.	Construct and explain the working of decimal adder?	Understand	CAEC020.8
10.	Design 2-digit BCD adder with the help of binary adders?	Understand	CAEC020.8
11.	Design Full Adder using NAND gates?	Understand	CAEC020.8
PART-B(1)(Long Answer Questions-CIE-II)			
12.	State the procedure to implement Boolean function using decoder and also mention the uses of decoders?	Understand	CAEC020.8
13.	Design Multiply 011_2 by 110_2 using binary multiplication method?	Understand	CAEC020.8
14.	Design a 2-bit Magnitude Comparator and draw the block diagram?	Understand	CAEC020.8
15.	Summarize the following Boolean function using 8:1 mux $F(A,B,C,D)=\pi M(0,3,5,8,9,10,12,14)$	Understand	CAEC020.8
16.	Design and implement a full adder circuit using a 3:8 decoder?	Understand	CAEC020.8

17.	Design Full Subtractor using NAND gates?	Understand	CAEC020.8
18.	Design FullSubtractor using NOR gates?	Understand	CAEC020.8
19.	Design Full Adder using NOR gates?	Understand	CAEC020.8
20.	Design 4 input Priority Encoder?	Remember	CAEC020.8
PART-C(Problem Solving Critical Thinking Questions -CIE-I)			
	Design a combinational logic circuit that produces the product of 2 binary number of following function $A=(A_1,A_0)*B=(B_1, B_0)$	Understand	CAEC020.8
2.	Solve the function using multiplexer $F(x,y,z)=\sum(0,2,6,7)$	Understand	CAEC020.8
3.	A combinational circuit has 4 inputs(A,B,C,D) and three outputs(X,Y,Z)XYZ represents a binary number whose value equals the number of 1's at the input: i. Find the minterm expansion for the X,Y,Z ii. Find the maxterm expansion for the Y and Z	Remember	CAEC020.8
4.	Design a combinational logic circuit with 4 inputs A, B, C, D. The output Y goes High if and only if A and C inputs go High. i. Draw the truth table. ii. Minimize the Boolean function using K-map. iii. Draw the circuit diagram?	Understand	CAEC020.8
5.	Design a logic circuit to convert excess-3 code to BCD code?	Understand	CAEC020.8
6.	Design a logic circuit to convert BCD code to XS-3 code?	Understand	CAEC020.8
PART-C(1)(Problem Solving Critical Thinking Questions -CIE-II)			
7.	Design a multiple circuit to multiply the following binary number $A=A_0A_1A_2A_3$ and $B=B_0B_1B_2B_3$ using required number of binary parallel adders?	Understand	CAEC020.8
8.	Solve the following Boolean functions using decoder and OR gates: $F_1(A,B,C,D)=\sum(2,4,7,9)$ $F_2(A,B,C,D)=\sum(10,13,14,15)$	Understand	CAEC020.8
9.	Solve the following Boolean functions using decoder and OR gates: $F_1(A,B,C,D)=\sum(3,5,6,8)$ $F_2(A,B,C,D)=\sum(11,12,13,15)$	Understand	CAEC020.8
10.	Solve the following Boolean function using 8:1multiplexer $F(A,B,C,D)=\sum m(1,3,5,7,8,9,0,2,13)$	Understand	CAEC020.8
11.	Solve the following Boolean function using 8:1 de- multiplexer $F(A,B,C,D)=\sum m(1,3,5,7,8,9,0,2,10,12,13)$	Understand	CAEC020.8
UNIT-IV DESIGN OF SEQUENTIAL CIRCUITS			
PART-A(Short Answer Questions)			
1.	Differentiate combinational and sequential logic circuits?	Remember	CAEC020.9
2.	Explain basic difference between a shift register and counter?	Remember	CAEC020.9
3.	Illustrate applications of shift registers?	Remember	CAEC020.12
4.	Define bidirectional shift register?	Remember	CAEC020.12
5.	Differentiate Flip-flop and latch?	Understand	CAEC020.12
6.	Define Counter?	Remember	CAEC020.12
7.	Classify the basic types of counters?	Remember	CAEC020.12
8.	Differentiate the advantages and disadvantages of ripple counters?	Remember	CAEC020.12
9.	Describe the applications of Counters?	Understand	CAEC020.12
10.	Design D-latch using NAND?	Remember	CAEC020.12
11.	Design and explain gated latch logic diagram?	Understand	CAEC020.12
12.	Define race around condition? How it can be avoided?	Remember	CAEC020.8

13.	Convert the following JK Flip Flop to using, i) SR ii) T iii) D	Remember	CAEC020.12
14.	Convert the following SR Flip-Flop to using, i) JK ii) D iii) T	Remember	CAEC020.12
15.	Explain what is a synchronous latch?	Remember	CAEC020.12
16.	Construct a latch using universal gates?	Remember	CAEC020.12
17.	Explain what do you mean a stable state?	Understand	CAEC020.12
18.	Define a Flip-Flop?	Remember	CAEC020.12
19.	Define applications of Flip-Flops?	Remember	CAEC020.12
20.	Explain what is meant by clocked flip-flop?	Remember	CAEC020.12
PART-B(Long Answer Questions)			
1.	Explain the design of Synchronous Sequential circuit with an example?	Remember	CAEC020.9
2.	Write short notes on shift register? Mention its application along with the Serial Transfer in 4-bit shift Registers?	Remember	CAEC020.9
3.	Explain about Binary Ripple Counter? What is MOD counter?	Remember	CAEC020.12
4.	Define BCD Counter and Draw its State table for BCD Counter?	Remember	CAEC020.12
5.	Explain the state reduction and state assignment in designing sequential circuit. Consider one example in the above process?	Remember	CAEC020.12
6.	Design a sequential circuit with two D flip-flops A and B. and one input x. When, x=0, the state of the circuit remains the same. When, x=1, the circuit goes through the state transition from 00 to 11 to 11 to 10 back to 00.andrepeats?	Remember	CAEC020.12
7.	Design a Modulo-12 up Synchronous counters using T-Flip Flops and draw the Circuit diagram for synchronous mod-12 counter?	Remember	CAEC020.12
8.	Explain the Ripple counter design. Also the decade counters design?	Remember	CAEC020.12
9.	Design a 3 bit ring counter? Discuss how ring counters differ from twisted ring counter?	Remember	CAEC020.12
10.	Design a Johnson counter?	Remember	CAEC020.12
11.	Design Johnson counters and state its advantages and disadvantages?	Remember	CAEC020.12
12.	Explain with the help of a block diagram, the basic components of a Sequential Circuit?	Remember	CAEC020.12
13.	Explain about RS and JK flip-flops with functional diagram and truth tables?	Remember	CAEC020.12
14.	Define T – Flip-flop with the help of a logic diagram and characteristic table?	Remember	CAEC020.12
15.	Define Latch. Explain about Different types of Latches in detail?	Remember	CAEC020.12
16.	Define JK – Flip-flop with the help of a logic diagram and characteristic table?	Remember	CAEC020.12
17.	List the characteristic equations for RS,JK,T and data Flip-Flops?	Remember	CAEC020.12
18.	Construct the transition table for the following flip-flops i) SRFF ii) ii) DFF	Remember	CAEC020.12
19.	Describe the steps involved in design of asynchronous sequential circuit in detail with an example?	Remember	CAEC020.12
20.	Differentiate Synchronous and Asynchronous counters?	Remember	CAEC020.12
PART-C(Problem Solving Critical Thinking Questions)			
1.	Explain the JK and Master slave Flip-flop? Give its timing waveform?	Remember	CAEC020.12

2.	A sequential circuit has 3 flip-flops, A,B and C and one input ,X it is described by the following flip flop input functions? $D_A=(BC^I+B^IC)x+(BC+B^IC^I)x^I$ $D_B=A$, $D_C=B$ i) Derive the state table for circuit ii) Draw two state diagrams: One for x=0 and for x=1	Remember	CAEC020.12
3.	Design and implement 4-bit binary counter (using D flip flops)which counts all possible odd numbers only?	Remember	CAEC020.12
4.	Design Moore Machine and draw state diagram and assignment?	Remember	CAEC020.13
5.	Design Mealy Machine and draw state diagram and assignment?	Remember	CAEC020.13
6.	Design a MOD-5 synchronous counter using flip flops and implement it? Also draw the timing diagram?	Remember	CAEC020.13
7.	Design a Ring counter using JK flip-flop?	Remember	CAEC020.12
8.	Design a Twisted Ring counter using JK flip-flop?	Remember	CAEC020.12
9.	Design MOD5 up and Down counter?	Remember	CAEC020.13
UNIT-V MEMORY			
PART-A(Short Answer Questions)			
1.	Explain what is PROM?	Understand	CAEC020.14
2.	Explain in detail about RAM and types of RAM?	Understand	CAEC020.14
3.	Illustrate the features of a ROM cell?	Understand	CAEC020.14
4.	Explain in detail about ROM and types of ROM?	Understand	CAEC020.14
5.	Explain is ROM is volatile Memory?	Understand	CAEC020.14
6.	Describe what is meant by memory expansion? Mention its limits?	Understand	CAEC020.14
7.	List a note on magnetic tape?	Understand	CAEC020.14
8.	State the advantages and disadvantages of magnetic tape and Magnetic disk?	Understand	CAEC020.15
9.	Differentiate static and dynamic RAM?	Understand	CAEC020.15
10.	Explain what is the use of cache memory?	Understand	CAEC020.14
11.	Design and explain the following mapping techniques of cache: a) Direct mapping b) Associative mapping	Understand	CAEC020.15
12.	Explain different replacement algorithms in detail?	Understand	CAEC020.14
13.	Explain what is EPROM?	Understand	CAEC020.15
14.	Differentiate between PROM and EPROM?	Understand	CAEC020.14
15.	Explain what is EEPROM?	Understand	CAEC020.15
16.	Explain what is PLA? Explain types of Programmable logic devices with examples?	Understand	CAEC020.14
17.	Explain the capacity of Programmable logic array specified in memory unit?	Understand	CAEC020.15
18.	Explain what are Programmable logic devices and explain in brief?	Understand	CAEC020.14
19.	Explain PLA with the help of block diagram?	Understand	CAEC020.15
20.	Explain the advantage of PROM over PLD?	Understand	CAEC020.14
PART-B(Long Answer Questions)			
1.	List How many address bits are needed to operate a 2 K *8 ROM?	Understand	CAEC020.15
2.	Construct a logic functional diagram of memory cell?	Understand	CAEC020.15
3.	Differentiate Static RAM cell with Dynamic RAM cell with functional diagrams?	Understand	CAEC020.15
4.	Explain the read and write operations of Random access memory	Understand	CAEC020.14

	and how can it perform?		
5.	Explain the operation of DRAM with suitable functional diagram and examples?	Understand	CAEC020.15
6.	Construct the signals of a 32*8 RAM with control input. Show the external connections necessary to have a 128*8 RAM using decoder and replication of this RAM?	Understand	CAEC020.14
7.	Implement 2-bit squaring time no of address lines and data lines used in ROM?	Understand	CAEC020.16
8.	Implement 2-bit multiplication time no of address lines and data lines used in ROM?	Understand	CAEC020.14
9.	Explain two ways set associative mapping and four way set associative mapping techniques with an example for each?	Understand	CAEC020.15
10.	Explain how a program gets executed faster using a cache memory?	Understand	CAEC020.14
11.	Design a BCD to Excess-3 code converter and implement using suitable PLA?	Understand	CAEC020.15
12.	Construct the block diagram of PLA. Which are the teams programmable? How inverter is useful in PLA construction atthe output?	Understand	CAEC020.14
13.	Sketch the PLA program table for the four Boolean functions. Minimize the number of product terms? $A(x,y,z)=\sum(0,1,3,5)$ $B(x,y,z)=\sum(2,6)$ $C(x,y,z)=\sum(1,2,3,5,7)$ $D(x,y,z)=\sum(0,1,6)$	Understand	CAEC020.15
14.	Sketch a PLA circuit to implement the logic functions $A^IBC+AB^IC+AC^I$ and $A^I B^I C^I +BC$.	Understand	CAEC020.14
15.	Explain in detail about various cache memory organizations?	Understand	CAEC020.16
16.	Sketch the ROM for the four Boolean functions. Minimize the number of product terms? $A(x,y,z)=\sum(1,2,4,7)$ $B(x,y,z)=\sum(0,1,3,5,6)$ $C(x,y,z)=\sum(0,2,4,5,7)$ $D(x,y,z)=\sum(3,5,6,7)$	Understand	CAEC020.15
17.	Explain the techniques used to perform the write operations in cache memory?	Understand	CAEC020.15
18.	Explain in detail about the operation of Static RAM cell?	Understand	CAEC020.15
19.	Differentiate PAL with PLA with following examples?	Understand	CAEC020.14
20.	"Memory hierarchy design is based on the principle of Locality of reference". Explain the principle?	Understand	CAEC020.15
PART-C(Problem Solving Critical Thinking Questions)			
1.	Solve the following two Boolean functions using a PLA having 3-inputs,4 product terms and 2 outputs? $F_1(A,B,C)=\sum(0,1,2,4)$ $F_2(A,B,C)=\sum(0,5,6,7)$	Understand	CAEC020.15
2.	Design 1k*8 RAM using two 1k*4 IC?	Understand	CAEC020.15
3.	Solve 2048*8 memories using 256*8 memory chip .Also show the memory address associated with each memory chip?	Understand	CAEC020.14
4.	Calculate the utilization factor of tape, if the gap length is 0.5in, the storage density S=3000 bytes/in and data storage capacity is 6kbytes?	Understand	CAEC020.15
5.	A two way set associative cache memory uses block of four words. The cache accommodates a total of 2048 words from main memory. The main memory size is128k*32	Understand	CAEC020.16

	i. Find how many bits are there in tag index, block and word field of address format? ii. Find the size of cache memory?		
6.	Solve the following multi Boolean function using 3*4*2 PLA PLD? $F_1(a_2, a_1, a_0)=\sum m(0,1,3,5)$ $F_2(a_2, a_1, a_0)=\sum m(3,5,7)$	Understand	CAEC020.15
7.	Design and implement 3-bit binary to gray code converter using PLA?	Understand	CAEC020.15
8.	Calculate the average access time of memory for a computer with cache access time of 100ns,a main memory access of1000ns and a hit ratio is 0.9?	Understand	CAEC020.16
9.	A direct mapped cache has the following parameters: cache size=1k words, Block size=128 words and main memory size is 64 k words. Find the number of bits in TAG, WORD and BLOCK in main memory address?	Understand	CAEC020.16
10.	Design a combinational circuit using PLA. The circuit accepts3-bit number and generates an output binary number equal to square of input number?	Understand	CAEC020.15

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