INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING
TUTORIAL QUESTION BANK

Course Name	:	**DIGITAL SYSTEM DESISN**
Course Code	:	**AEC002**
Class	:	**B. Tech III Semester**
Regulation	:	**IARE-R16**
Branch	:	**ECE**
Academic Year	:	**2018– 2019**
Course Coordinator	:	**Dr. K.Nehru Professor, ECE**
Course Faculty	:	**Dr.Lalith Kumar Kaul , Professor, ECE** **Dr.P.Munaswamy, Professor, ECE** **Mr. K.Arun sai, Assistant Professor, ECE**

I. COURSE OBJECTIVES:

The course should enable the students to:

S. NO	DESCRIPTION
I	Formulate and solve problems involving number systems and operations related to them and generate different digital codes. .
II	Describe and analyze functions of logic gates and optimize the logic functions using K -map and Quine - McClusky methods.
III	Demonstrate knowledge of combinational and sequential logic circuits elements like Adders, Multipliers, flip-flops and use them in the design of latches, counters, sequence detectors, and similar circuits
IV	Design a simple finite state machine from a specification and be able to implement this in gates and edge triggered flip-flops

II. COURSE LEARNING OUTCOMES:

Students, who complete the course, will have demonstrated the ability to do the following:

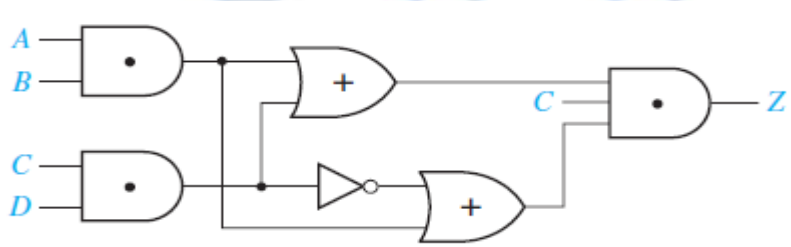
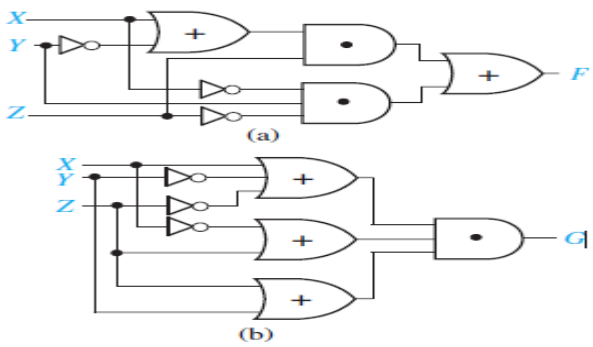
CAEC002.01	Understand number systems, binary addition and subtraction, 2's complement representation and operations with this representation and understand the different binary codes.
CAEC002.02	Illustrate the switching algebra theorems and apply them for reduction of Boolean function.
CAEC002.03	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
CAEC002.04	Discuss about digital logic gates and their properties, and implement logic gates using universal gates.
CAEC002.05	Evaluate functions using various types of minimizing algorithms like Boolean algebra.
CAEC002.06	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method
CAEC002.07	Design Gate level minimization using K-Maps and realize the Boolean function using logic gates.
CAEC002.08	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder.
CAEC002.09	Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.
CAEC002.10	Analyze and apply the design procedures of small sequential circuits to build the gated latches.

CAEC002.11	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.
CAEC002.12	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
CAEC002.13	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
CAEC002.14	Understand and analyze the design of a finite state machine and implement Moore and Mealy machine.
CAEC002.15	Understand and analyze the merger chart methods like merger graphs, merger table for completely and incompletely specified machines.
CAEC002.16	Apply the concept of digital logic circuits to understand and analyze real time applications.
CAEC002.17	Acquire the knowledge and develop capability to succeed national and international level competitive examinations.

TUTORIAL QUESTION BANK

S. No	Question	Blooms Taxonomy Level	Course Learning Outcome
	UNIT-I FUNDAMENTALS OF DIGITAL TECHNIQUES		
PART-A (SHORT ANSWER QUESTIONS)			
1	Write short notes on binary number systems.	Remember	CAEC002.01
2	Discuss 1's and 2's complement methods of subtraction.	Understand	CAEC002.01
3	Discuss octal number system.	Understand	CAEC002.01
4	Convert the octal numbers into binary, decimal and Hexadecimal numbers $(45.5)_8$, $(32.2)_8$.	Remember	CAEC002.01
5	Show an example to convert gray code to binary code.	Understand	CAEC002.01
6	Describe a short note on four bit BCD codes.	Remember	CAEC002.01
7	Illustrate about unit –distance code? State where they are used.	Understand	CAEC002.01
8	List the applications of error correcting codes.	Remember	CAEC002.01
9	Convert 10101101.0111 to octal equivalent and hexadecimal equivalent.	Understand	CAEC002.01
10	Prove that negative logic of NOR gate is equivalent to positive logic of AND gate	Remember	CAEC002.01
11	Identify Y for a given problem is $(2.3)_8 + (1.7)_8 = (Y)_8$.	Understand	CAEC002.01
12	Give the examples of unit distance codes	Remember	CAEC002.01
13	Convert $(4085)_8$ into base 5.	Understand	CAEC002.01
14	Convert $(4085)_8$ into base 3.	Remember	CAEC002.01
15	Solve subtraction between 9 - 5 using xs-3.	Remember	CAEC002.01
PART-B (LONG ANSWER QUESTIONS)			
1	Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend. i. 100 – 110000 ii. 11010 - 1101.	Understand	CAEC002.01
2	Perform arithmetic operation indicated below. Follow signed bit notation. i. 001110 + 110010 ii. 101011 - 100110.	Remember	CAEC002.01
3	Find $(3250 - 72532)_{10}$ using 10's complement	Understand	CAEC002.01
4	State 819+54 1 using XS-3 and BCD.	Remember	CAEC002.01
5	(a) Add 01100100 by 00011001. (b) Given that $(292)_{10} = (1204)_b$ determine `b'.	Understand	CAEC002.01
6	(a) What is the gray code equivalent of the Hex Number 3A7. (b) Find 9's complement of $(25.639)_{10}$.	Remember	CAEC002.01
7	(a) Find (72532 - 03250) using 9's complement. (b) Show the weights of three different 4 bit self complementing codes whose only negative weight is - 4 and write down number system from 0 to 9.	Understand	CAEC002.01
8	Explain Self complemented codes.	Understand	CAEC002.01
9	Convert $(4085)_{10}$ into base-4 and obtain its 9's complement.	Remember	CAEC002.01
10	Convert the following Hexadecimal number to their Decimal equivalent $(EAF1)_{16}$.	Understand	CAEC002.01
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)			
1	Given the 8bit data word 01011011, generate the 12 bit composite word for the hamming code that corrects and detects single errors.	Remember	CAEC002.01
2	Write the first 20 decimal digits in base 3 and base 16.	Understand	CAEC002.01
3	A device transmits the binary data using even parity, the message is 1011001. Identify the receiver receives the correct data or not.	Remember	CAEC002.01
4	Subtract the following binary numbers using 1's complement. i) 1011-101 ii) 10110-1011	Remember	CAEC002.01
5	Differentiate between BCD code and 2421 code and XS-3.	Understand	CAEC002.01
6	Find 7 bit hamming code for given message 1010 by using odd parity.	Understand	CAEC002.01

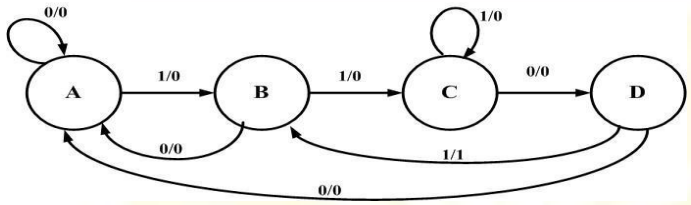
S. No	Question	Blooms Taxonomy Level	Course Learning Outcome
7	The message below coded in the seven bit hamming code is transmitted through a noisy channel. Decode the message assuming the at most a single error occurred in each code word,1001011,0111001,1110110.	Remember	CAEC002.01
8	Generate an 11 bit hamming code for a given data 1011010 using odd parity.	Remember	CAEC002.01
9	Solve Subtraction and Addition 4327 and 1562 using BCD and Xs-3 Method.	Understand	CAEC002.01
10	Generate the weighted codes for the decimal digits using the weights i) 3,3,2,1 ii) 2,4,2,1	Understand	CAEC002.01
	UNIT-II BOOLEAN ALGEBRA AND THEOREMS		
PART-A(SHORT ANSWER QUESTIONS)			
1	Simplify F = ∑ m (0,1,2) using 2 variable Karnaugh map.	Remember	CAEC002.06
2	Define Implicant, Prime Implicant and Essential Prime Implicant.	Understand	CAEC002.06
3	Define Consensus Theorem.	Remember	CAEC002.05
4	Solve AB^1+BC+CA=AB+BC.	Remember	CAEC002.02
5	Simplify the Boolean function A′BC +A′BC′ + AB′C′ + AB′C using K-map.	Understand	CAEC002.06
6	Define three inputs NAND gate and sketch the symbol.	Remember	CAEC002.04
7	Define three inputs NOR gate and sketch the symbol.	Understand	CAEC002.04
8	Define the importance of prime implications.	Understand	CAEC002.06
9	Locate the minters in a three variable map for f=∑m (0, 1, 5, 7).	Remember	CAEC002.03
10	Simplify the Boolean function x′yz + x′yz′ + xy′z′ + xy′z without using K-Map.	Understand	CAEC002.05
11	Design 2 input XOR gate using minimum number of NAND gates.	Understand	CAEC002.03
12	Reduce the Boolean function xyz + xyz′ + x′y′z′ + xy′z′ without using K- Map.	Remember	CAEC002.03
13	List the truth table of XOR and XNOR gates.	Remember	CAEC002.03
14	Simplify the function X+XY+Y using NOR gates.	Understand	CAEC002.03
15	Sketch and implement following logic function using k-map for given Y(A,B,C,D)= ∑m(0,1,2,3,4,7,8,9,10,11,12,14).	Remember	CAEC002.03
PART-B (LONG ANSWER QUESTIONS)			
1	Minimize the following function using K-map. F (A, B, C, D) = ∑m (1, 3, 5, 7, 9, 10, 11, 12, 15).	Remember	CAEC002.06
2	Minimize the following function using K-map f = ∑m (1, 2, 3, 5, 12, 13).	Remember	CAEC002.06
3	Simplify the following Boolean expressions using K-map and implement them using logic gates. (a) F (A, B, C, D) = AB'C' + AC + A'CD'. (b) F (W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ.	Understand	CAEC002.05
4	Minimize the following function using K-map. F (A, B, C, D,E) = ∑m (1,3,5,7,9,10,11,12,15,19,21,22,27) + ∑d (0,4,8).	Understand	CAEC002.06
5	Minimize the Boolean function F (w, x, y, z) = Σm (1, 3, 7, 11, 15) + Σd (0, 2, 5) using sum of product and product of sum forms.	Remember	CAEC002.06
6	Reduce the following expression using Karnaugh map (B 'A + A'B + AB').	Understand	CAEC002.06
7	Show that AB+AB'C+BC' = AC+BC'.	Remember	CAEC002.02
8	Convert (A+B)(A+B+C)(B+C) into canonical POS and SOP forms.	Understand	CAEC002.04
9	Expand the Boolean function F= A (A'+B) (A'+B+C') to maxterms and minterms.	Remember	CAEC002.04
10	Identify all the prime implicants and essential prime implicants for a given function using k-map. F(A,B,C,D) = Σm (0,1,2,5,6,7,8,9,10,13,14,15).	Remember	CAEC002.06
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)			
1	Implement the Boolean function F = AB + CD + E using NAND gates only.	Understand	CAEC002.04
2	Simplify the Boolean function F(w, x, y, z) = Σm(1, 3, 7, 11, 15) + Σd (0, 2, 5).	Remember	CAEC002.06

S. No	Question	Blooms Taxonomy Level	Course Learning Outcome
3	Design a 3 input majority gate using NAND gates.	Understand	CAEC002.04
4	Design a half adder using NOR gates.	Understand	CAEC002.04
5	A function having three data inputs to implement the logic for the function F = Σm (0, 1, 2, 3, 4, 7) using Boolean expression and verify the function using Karnaugh map.	Remember	CAEC002.06
6	Identify all the prime implicants and essential prime implicants of the following functions Using K-Map. F(A,B,C,D) = Σm (0,1,2,5,6,7,8,9,10,13,14,15).	Remember	CAEC002.06
7	Simplify the following circuit to a single gate: 	Remember	CAEC002.02
8	Simplify the Boolean function F = Σm (0, 1, 2, 3, 4, 7, 9, 10, 14, 15) using tabular method.	Understand	CAEC002.06
9	Show that the following two gate circuits realize the same function. 	Understand	CAEC002.02
10	Convert (A+B+C)(B+C')(A'+C) into standard POS format.	Understand	CAEC002.03
	UNIT-III DESIGN OF COMBINATIONAL CIRCUITS		
PART-A(SHORT ANSWER QUESTIONS)			
1	What do you mean by adder circuit.	Remember	CAEC002.08
2	State the truth table for 1 bit half adder.	Remember	CAEC002.08
3	Design a logic circuit to convert BCD and gray code.	Understand	CAEC002.08
4	Design Full adder using Logic Gates.	Understand	CAEC002.08
5	Design Half subtractor using NAND Gates.	Remember	CAEC002.08
6	Design a Full adder using NAND Gates.	Understand	CAEC002.08
7	Design a Full adder using NOR Gates.	Remember	CAEC002.08
8	Design Half subtractor using NOR Gates.	Remember	CAEC002.08
9	Design a Full subtractor using NAND Gates.	Understand	CAEC002.08
10	Design a Full subtractor using NOR Gates.	Remember	CAEC002.08
11	Design a full adder using two half adders.	Remember	CAEC002.08
12	State the truth table for 1 bit full adder.	Understand	CAEC002.08

S. No	Question	Blooms Taxonomy Level	Course Learning Outcome
13	State the truth table for 1 bit half subtractor.	Understand	CAEC002.08
14	State the truth table for 1 bit full subtractor.	Remember	CAEC002.08
15	Mention the design rules of combinational circuit.	Understand	CAEC002.08
CIE II			
1	Differentiate a parallel adder from serial adder.	Understand	CAEC002.08
2	Explain the working of a serial adder with the help of a block diagram.	Remember	CAEC002.08
3	Implement a 4-bit ripple adder using half-adder(s)/full-adder(s).	Understand	CAEC002.08
4	Realize a carry-look-ahead adder.	Remember	CAEC002.08
5	Explain a parallel adder/ subtractor using 2's complement system with the help of a logic diagram.	Remember	CAEC002.08
6	Explain the working of a BCD adder.	Understand	CAEC002.08
7	What is a ripple-carry-adder.	Remember	CAEC002.08
8	What is a serial adder.	Remember	CAEC002.08
9	Discuss why serial adders slower than parallel adders.	Understand	CAEC002.08
10	Explain how the look-ahead-carry adder speeds up the addition process.	Understand	CAEC002.08
11	What do you mean by carry look ahead adder.	Understand	CAEC002.08
12	Why parallel adder is faster than serial adder.	Remember	CAEC002.08
13	State the importance of control signal in 2's complement adder circuit.	Remember	CAEC002.08
14	Give the examples for combinational circuits.	Understand	CAEC002.08
15	Give the circuit for serial adder circuit.	Remember	CAEC002.08
PART-B(LONG ANSWER QUESTIONS)			
1	Design 4 bit parallel adder using full adders.	Remember	CAEC002.08
2	Design a full adder using two half adders and OR gate.	Understand	CAEC002.08
3	Design a 4-bit Binary Adder using full adder.	Remember	CAEC002.08
4	Explain the working of carry look-ahead generator.	Remember	CAEC002.08
5	Design a combinational circuit that generates the 9's complement of BCD digit.	Understand	CAEC002.08
6	Design a combinational circuit that generates logic '1' for odd inputs.	Understand	CAEC002.08
7	Explain the design procedure for code converter with the help of example.	Remember	CAEC002.08
8	Design a logic circuit to convert gray code to binary code.	Remember	CAEC002.08
9	Design a logic circuit to convert binary code to gray code.	Understand	CAEC002.08
10	Design a logic circuit to convert BCD code to binary code.	Understand	CAEC002.08
CIE II			
1	Design a combinational circuit to find the 2's complement of given binary number and realize using NAND gates.	Understand	CAEC002.08
2	Design a combinational circuit to perform the 1's complement subtractor.	Understand	CAEC002.08
3	Design circuit to detect odd number for 3 bit binary number.	Understand	CAEC002.08
4	Design circuit to detect even number for 4 bit binary number.	Remember	CAEC002.08
5	Design a combinational circuit to perform the 2's complement subtractor.	Remember	CAEC002.08
6	Design carry look ahead adder.	Understand	CAEC002.08
7	Design 2-digit BCD adder with the help of binary adders.	Remember	CAEC002.08
8	Design 1-digit BCD adder with the help of binary adders.	Remember	CAEC002.08
9	Illustrate the principle of BCD adder.	Understand	CAEC002.08
10	Differentiate serial adder and parallel adder.	Remember	CAEC002.08
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)			
1	Design a 4-bit Combinational circuit which generates the output as 2's complement of input binary number.	Remember	CAEC002.08
2	Design a combinatorial circuit that converts a decimal digit from 2,4,2,1 code to the 8,4,2,1 code?	Understand	CAEC002.08
3	Design a combinatorial circuit that accepts a three bit number and generates an output Binary number equal to the square of the input number.	Understand	CAEC002.08

S. No	Question	Blooms Taxonomy Level	Course Learning Outcome
4	Design a 4-bit Combinational circuit which generates the output as 1's complement of input binary number.	Remember	CAEC002.08
5	Construct and explain the working of decimal adder.	Understand	CAEC002.08
6	Realize the Boolean expression for full subtractor.	Understand	CAEC002.08
7	Design half adder using AND & OR gates.	Remember	CAEC002.08
8	Realize the Boolean expression for half subtractor.	Understand	CAEC002.08
9	Design a combinatorial circuit that accepts a three bit number and generates an output Binary number equal to the cube of the given input number.	Understand	CAEC002.08
10	Implement the circuit to produce the octal number for given 4 bit binary number.	Remember	CAEC002.08
	CIE II		
1	Design 4-digit BCD adder with the help of binary adders.	Understand	CAEC002.08
2	Design 3 bit binary to XS-3 code.	Remember	CAEC002.08
3	A combinational circuit has 4 inputs(A,B,C,D) and three outputs(X,Y,Z) XYZ represents a binary number whose value equals the number of 1's at the input: i. Find the minterm expansion for the X,Y,Z. ii. Find the maxterm expansion for the Y and Z.	Understand	CAEC002.08
4	Design a combinational logic circuit with 4 inputs A, B, C, D. The output Y goes High if and only if A and C inputs go High. Draw the truth table. Minimize the Boolean function using K-map. Draw the circuit diagram.	Remember	CAEC002.08
5	Design a logic circuit to convert excess-3 code to BCD code.	Understand	CAEC002.08
6	Design and implement a 4 bit binary serial adder using three full adders and one half adders? State how many full adders and half adders are required to design n –bit binary serial adder?	Remember	CAEC002.08
7	Design carry look ahead adder circuit with suitable problem.	Remember	CAEC002.08
8	Implement a 2's complement addition and subtraction using parallel adders.	Understand	CAEC002.08
9	Design a 2's complement addition and subtraction using parallel adders.	Understand	CAEC002.08
10	Design a combinatorial circuit that converts a decimal to binary code.	Remember	CAEC002.08
	UNIT-IV SEQUENTIAL CIRCUITS		
	PART-A (SHORT ANSWER QUESTIONS)		
1	List the types of Shift registers.	Remember	CAEC002.11
2	Distinguish between a shift register and counter.	Understand	CAEC002.11
3	Illustrate the applications of shift registers.	Remember	CAEC002.11
4	Discuss about a bidirectional shift register.	Understand	CAEC002.11
5	Summarize about a dynamic shift register.	Understand	CAEC002.11
6	What do you mean by a stable state?	Remember	CAEC002.09
7	Define Flip-Flop and sketch the NAND Latch.	Understand	CAEC002.09
8	List out the applications of Flip-Flops.	Remember	CAEC002.09
9	Express your view about synchronous latch.	Understand	CAEC002.09
10	Why a gated D latch is called a transparent latch.	Remember	CAEC002.09
11	Construct the D latch using NAND.	Remember	CAEC002.09
12	Construct the D latch using NOR.	Understand	CAEC002.09
13	State the truth table for JK flip-flop.	Remember	CAEC002.09
14	State the truth table for SR flip-flop.	Understand	CAEC002.09
15	State the truth table for T flip-flop.	Understand	CAEC002.09
	PART-B (LONG ANSWER QUESTIONS)		
1	Implement a master slave flip flop with timing diagrams.	Understand	CAEC002.09
2	Explain Serial Transfer in 4-bit shift Registers.	Remember	CAEC002.11
3	Design a 4 bit ripple counter using JK flip flop.	Understand	CAEC002.13

S. No	Question	Blooms Taxonomy Level	Course Learning Outcome
4	Explain the operation of NAND and NOR based SR latch.	Remember	CAEC002.09
5	Differentiate combinational and sequential circuits.	Understand	CAEC002.10
6	Describe about T – Flip-flop with the help of a logic diagram and characteristic table. Derive a T-flip-flop from JK and D flip-flops.	Understand	CAEC002.09
7	Design a Modulo-12 up Synchronous counter using T-Flip Flops and draw the Circuit diagram.	Remember	CAEC002.09
8	Explain the Ripple counter design. Also a decadecounter design.	Remember	CAEC002.13
9	Write short notes on shift register? Mention its applications.	Remember	CAEC002.11
10	Design a left shift and right shift for the following data 10110101.	Understand	CAEC002.11
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)			
1	Explain the operation of SR Flip-Flop using asynchronous inputs with truth table.	Remember	CAEC002.09
2	Explain the Flip-Flop operating characteristics in detail	Remember	CAEC002.09
3	Draw the schematic circuit of an edge triggered flip-flop with “active low preset” and “active low clear” using NAND gats and explain its operation.	Understand	CAEC002.09
3	Convert a JK FF to i) SR ii) T iii) D	Understand	CAEC002.09
5	Design mod 10 synchronous counter.	Remember	CAEC002.12
6	Design Johnson counter using JK flip flops.	Understand	CAEC002.12
7	Design 3 bit asynchronous counter using SR flip flop.	Remember	CAEC002.13
8	Design 4 bit synchronous counter using t flip flop.	Remember	CAEC002.12
9	Give the transition table for the following flip-flops, i. SR FF ii. D FF.	Understand	CAEC002.09
10	Give the transition table for the following flip-flops, i. JK FF ii. T FF.	Remember	CAEC002.09
UNIT-V CAPABILITIES AND MINIMIZATION OF SEQUENTIAL MACHINES			
PART-A(SHORT ANSWER QUESTIONS)			
1	Indicate the capabilities and limitations of FSM.	Understand	CAEC002.14
2	Demonstrate about successor.	Understand	CAEC002.14
3	Describe about terminal state.	Understand	CAEC002.14
4	Define Moore machine.	Remember	CAEC002.14
5	Write the difference between Moore and Mealy machine.	Remember	CAEC002.14
6	State ‘state equivalence theorem’.	Understand	CAEC002.14
7	Define state assignment.	Remember	CAEC002.14
8	Define state compatibility.	Understand	CAEC002.14
9	Describe a Merger graph.	Understand	CAEC002.15
10	Explain about Merger table with example.	Remember	CAEC002.15
11	Define Mealy machine.	Remember	CAEC002.15
12	State the importance of subgraph.	Understand	CAEC002.15
13	State the importance of compatibility graph.	Understand	CAEC002.15
14	Write the importance of minimal cover table.	Remember	CAEC002.15
15	Define closed subgraph and write the importance of subgraph in FSM.	Understand	CAEC002.15
PART-B(LONG ANSWER QUESTIONS)			
1	Explain the design of Sequential circuit with an example. Show the state reduction, state assignment.	Remember	CAEC002.14
2	Define BCD Counter and Draw its State table for BCD Counter.	Remember	CAEC002.14
3	Explain the state reduction and state assignment in designing sequential circuit. Consider one example in the above process.	Understand	CAEC002.14
4	Design a sequential circuit with two D flip-ops A and B. and one input x.	Understand	CAEC002.14

<table>
<tr><th>S. No</th><th>Question</th><th>Blooms Taxonomy Level</th><th>Course Learning Outcome</th></tr>
<tr><td></td><td>when x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transition from 00 to 11 to 11 to 10 back to 00.and repeats.</td><td></td><td></td></tr>
<tr><td>5</td><td>Define Mealy machine and explain with an example.</td><td>Remember</td><td>CAEC002.14</td></tr>
<tr><td>6</td><td>Define Moore machine and explain with an example.</td><td>Understand</td><td>CAEC002.14</td></tr>
<tr><td>7</td><td>Explain about Merger Graph with example.</td><td>Understand</td><td>CAEC002.15</td></tr>
<tr><td>8</td><td>Consider an example for completely specified method and explain.</td><td>Remember</td><td>CAEC002.15</td></tr>
<tr><td>9</td><td>Explain about Partition Method with an example.</td><td>Understand</td><td>CAEC002.15</td></tr>
<tr><td>10</td><td>Write the differences between Mealy and Moore type machines with an example.</td><td>Remember</td><td>CAEC002.14</td></tr>
<tr><td colspan="4">PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)</td></tr>
<tr><td>1.</td><td>Draw the state table and state assignment for given state diagram
 
</td><td>Remember</td><td>CAEC002.14</td></tr>
<tr><td>2</td><td>For the machine given. Find the equivalence partition and a corresponding reduced machine in standard form? Explain?
<table>
<tr><th rowspan="2">PS</th><th colspan="2">NS,Z</th></tr>
<tr><th>X=0</th><th>X=1</th></tr>
<tr><td>A</td><td>E,0</td><td>D,1</td></tr>
<tr><td>B</td><td>F,0</td><td>D,0</td></tr>
<tr><td>C</td><td>E,0</td><td>B,1</td></tr>
<tr><td>D</td><td>F,0</td><td>B,0</td></tr>
<tr><td>E</td><td>C,0</td><td>F,1</td></tr>
<tr><td>F</td><td>B,0</td><td>C,0</td></tr>
</table></td><td>Understand</td><td>CAEC002.15</td></tr>
<tr><td>3</td><td>Design State diagram for given state table
<table>
<tr><th rowspan="2">PS</th><th colspan="2">NS</th><th colspan="2">Output</th></tr>
<tr><th>X=0</th><th>X=1</th><th>X=0</th><th>X=1</th></tr>
<tr><td>A</td><td>A</td><td>B</td><td>0</td><td>0</td></tr>
<tr><td>B</td><td>A</td><td>C</td><td>0</td><td>0</td></tr>
<tr><td>C</td><td>D</td><td>C</td><td>0</td><td>0</td></tr>
<tr><td>D</td><td>A</td><td>B</td><td>0</td><td>1</td></tr>
</table></td><td>Understand</td><td>CAEC002.15</td></tr>
</table>

<table>
<tr><th>S. No</th><th>Question</th><th>Blooms Taxonomy Level</th><th>Course Learning Outcome</th></tr>
<tr><td>4</td><td>Design a Merger graph and simplified graph for the given state table
<table>
<tr><th rowspan="2">PS</th><th colspan="4">NS,Z</th></tr>
<tr><th>I1</th><th>I2</th><th>I3</th><th>I4</th></tr>
<tr><td>A</td><td>…</td><td>E,1</td><td>B,1</td><td>….</td></tr>
<tr><td>B</td><td>…</td><td>D,1</td><td>…</td><td>F,1</td></tr>
<tr><td>C</td><td>F,1</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>D</td><td>…</td><td>…</td><td>C,1</td><td>…</td></tr>
<tr><td>E</td><td>C,0</td><td>…</td><td>A,0</td><td>F,1</td></tr>
<tr><td>F</td><td>D,0</td><td>A,1</td><td>B,0</td><td>…</td></tr>
</table></td><td>Understand</td><td>CAEC002.15</td></tr>
<tr><td>5</td><td>Draw the merger graph and obtain the set of maximal compatabilities for the incompletely specified sequential machine.
<table>
<tr><th rowspan="2">PS</th><th colspan="4">NS, Z</th></tr>
<tr><th>00</th><th>01</th><th>11</th><th>10</th></tr>
<tr><td>A</td><td>E,0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>B</td><td>-</td><td>F,1</td><td>E,1</td><td>A,1</td></tr>
<tr><td>C</td><td>F,0</td><td>-</td><td>A,0</td><td>F,1</td></tr>
<tr><td>D</td><td>-</td><td>-</td><td>A,1</td><td>-</td></tr>
<tr><td>E</td><td>-</td><td>C,0</td><td>B,0</td><td>D,1</td></tr>
<tr><td>F</td><td>C,0</td><td>C,1</td><td>-</td><td>-</td></tr>
<tr><td>G</td><td>E,0</td><td>-</td><td>-</td><td>A,1</td></tr>
</table></td><td>Understand</td><td>CAEC002.15</td></tr>
<tr><td>6</td><td>Draw the merger graph and obtain the set of maximal compatabilities for the completely specified sequential machine.
<table>
<tr><th rowspan="2">PS</th><th colspan="2">NS,Z</th></tr>
<tr><th>X=0</th><th>X=1</th></tr>
<tr><td>S1</td><td>S3,0</td><td>S2,0</td></tr>
<tr><td>S2</td><td>S2,0</td><td>S3,0</td></tr>
<tr><td>S3</td><td>S3,1</td><td>S2,0</td></tr>
</table></td><td>Remember</td><td>CAEC002.15</td></tr>
<tr><td>7</td><td>Draw the merger graph and obtain the set of maximal compatabilities for the incompletely specified sequential machine.
<table>
<tr><th rowspan="2">PS</th><th colspan="4">NS,Z</th></tr>
<tr><th>I1</th><th>I2</th><th>I3</th><th>I4</th></tr>
<tr><td>S1</td><td>S3,0</td><td>S1,-</td><td>-</td><td>-</td></tr>
<tr><td>S2</td><td>S6,-</td><td>S2,0</td><td>S1,-</td><td>-</td></tr>
<tr><td>S3</td><td>-,1</td><td>-,-</td><td>S4,0</td><td>-</td></tr>
<tr><td>S4</td><td>S1,0</td><td>-,-</td><td>-</td><td>S4,1</td></tr>
</table></td><td>Understand</td><td>CAEC002.15</td></tr>
</table>

<table>
<tr><th>S. No</th><th>Question</th><th>Blooms Taxonomy Level</th><th>Course Learning Outcome</th></tr>
<tr><td>8</td><td>Draw the merger graph and obtain the set of maximal compatabilities for the completely specified sequential machine.
<table>
<tr><th rowspan="2">PS</th><th colspan="2">NS,Z</th></tr>
<tr><th>X=0</th><th>X=1</th></tr>
<tr><td>A</td><td>E,0</td><td>D,1</td></tr>
<tr><td>B</td><td>F,0</td><td>D,0</td></tr>
<tr><td>C</td><td>E,0</td><td>B,1</td></tr>
<tr><td>D</td><td>F,0</td><td>B,0</td></tr>
<tr><td>E</td><td>C,0</td><td>F,1</td></tr>
<tr><td>F</td><td>B,0</td><td>C,0</td></tr>
</table></td><td>Understand</td><td>CAEC002.15</td></tr>
<tr><td>9</td><td>Draw the merger graph and obtain the set of maximal compatabilities for the incompletely specified sequential machine.
<table>
<tr><th rowspan="2">PS</th><th colspan="4">NS,Z</th></tr>
<tr><th>I1</th><th>I2</th><th>I3</th><th>I4</th></tr>
<tr><td>S1</td><td>S3,0</td><td>S1,-</td><td>-</td><td>-</td></tr>
<tr><td>S2</td><td>S6,-</td><td>S2,0</td><td>S1,-</td><td>-</td></tr>
<tr><td>S3</td><td>-,1</td><td>-,-</td><td>S4,0</td><td>-</td></tr>
<tr><td>S4</td><td>S1,0</td><td>-,-</td><td>-</td><td>S5,1</td></tr>
<tr><td>S5</td><td>-,-</td><td>S5,-</td><td>S2,1</td><td>S1,1</td></tr>
<tr><td>S6</td><td>-,-</td><td>S2,1</td><td>S6,-</td><td>S4,1</td></tr>
</table></td><td>Remember</td><td>CAEC002.15</td></tr>
<tr><td>10</td><td>Draw the merger graph and obtain the set of maximal compatabilities for the incompletely specified sequential machine.
<table>
<tr><th rowspan="2">PS</th><th colspan="2">NS,Z</th></tr>
<tr><th>X=0</th><th>X=1</th></tr>
<tr><td>S1</td><td>S3,0</td><td>S2,0</td></tr>
<tr><td>S2</td><td>S2,-</td><td>S3,0</td></tr>
<tr><td>S3</td><td>S3,1</td><td>S2,0</td></tr>
</table></td><td>Understand</td><td>CAEC002.15</td></tr>
</table>

HOD, ECE