INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Name	**:**	**PULSE AND DIGITAL CIRCIUTS**
Course Code	**:**	**AEC006**
Class	**:**	**B. Tech IV Semester**
Branch	**:**	**ECE**
Academic Year	**:**	**2018– 2019**
Course Coordinator	**:**	**Mr. B Naresh, Assistant professor, Dept. of ECE.**
Course Faculty	**:**	**Ms. J Swetha, Assistant professor** **Ms. N Anusha, Assistant professor** **Mr. S Lakshmana Chary, Assistant professor** **Mr. B Naresh, Assistant professor**

COURSE OBJECTIVES:

The course should enable the students to:

S. NO	DESCRIPTION
I	Proficient in the use of linear and non linear wave shaping circuits for sinusoidal, pulse and ramp inputs.
II	Construct various multivibrators using transistors, and design sweep circuits and sampling gates
III	Evaluate the methods to achieve frequency synchronization and division using uni-junction transistors, multivibrators and symmetric circuits.
IV	Realize logic gates using diodes and transistors and distinguish between various logic families.

COURSE LEARNING OUTCOMES:

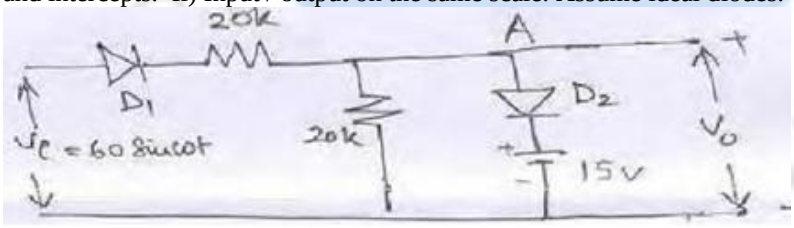
Students, who complete the course, will have demonstrated the ability to do the following:

CAEC006.01	Understand the response of high pass RC and low pass RC circuits to different non sinusoidal inputs with different time constants and identify RC circuit's applications.
CAEC006.02	Discuss the various clipper circuits using switching components like diodes, transistors and design various clipper circuits with and without reference voltages.
CAEC006.03	Formulate clamping circuit theorem and design practical clamping circuits by understanding the different diode clamper circuits
CAEC006.04	apply design procedures to different bistable multivibrator circuits by Understanding the Bistable multi with triggering methods and
CAEC006.05	Evaluate triggering points, hysteresis width of Schmitt trigger circuit and also design practical Schmitt trigger circuit.
CAEC006.06	Understand the Monostable, Astable multi circuits with applications and evaluate time, frequency parameters.
CAEC006.07	Understand the different types of sampling gates with operating principles using diodes, transistors and also evaluate different parameters of sampling gates.
CAEC006.08	Implement different methods to generate time base waveforms using various sweep circuits like Bootstrap and Miller circuits.
CAEC006.09	Apply the various time base generator circuits in applications like cathode ray oscilloscope and television.
CAEC006.10	Understand the concept of frequency division, synchronization and pulse synchronization of various Relaxation circuits.
CAEC006.11	Analyze the frequency division with sweep circuits and various relaxation circuits like Astable multi, Monostable multi circuits.

CAEC006.12	Implement the synchronization of different sweep circuits with symmetrical signals and sinusoidal signals.
CAEC006.13	Understand and analyze the different bipolar, unipolar logic families like DTL, RTL, DCTL, TTL, MOS and CMOS.
CAEC006.14	Evaluate the specifications of logic families such as propagation delay, fan in, fan out, noise immunity and compare various logic families.
CAEC006.15	Understand and analyze the tri state logic and interfacing of TTL and CMOS logic families.
CAEC006.16	Apply the concept of pulse and digital circuits to understand and analyze real time applications.
CAEC006.17	Acquire the knowledge and develop capability to succeed national and international level competitive examinations.

TUTORIAL QUESTION BANK

S. No	Questions	Blooms Taxonomy Level	Course learning Outcome
UNIT-I			
WAVE SHAPING CIRCUITS			
PART-A (SHORT ANSWER QUESTIONS)			
1	Name the signals which are commonly used in pulse circuits and define any five of them.	Remember	CAEC006.01
2	Define linear wave shaping.	Remember	CAEC006.01
3	Explain the fractional tilt of a high pass RC circuit.	Remember	CAEC006.01
4	State the lower 3-db frequency of high-pass circuit.	Remember	CAEC006.01
5	Distinguish between the linear and non-linear wave shaping circuits.	Understand	CAEC006.01
6	Show that a high pass circuit with a small time constant acts as differentiator.	Remember	CAEC006.01
7	Define Rise time. Give the relations between rise time and bandwidth of Low Pass RC circuit.	Remember	CAEC006.01
8	Show that a low pass circuit with a time constant acts as Integrator.	Remember	CAEC006.01
9	State the output voltage for low pass RC circuit under step input.	Understand	CAEC006.01
10	Define non-linear wave shaping. List out the names of nonlinear wave shaping.	Remember	CAEC006.01
11	Define Series clipper and shunt clipper.	Remember	CAEC006.02
12	Describe the relationship between R and the forward resistance R_f and reverse resistance R_r of the Clipping Circuit.	Understand	CAEC006.02
13	Describe clamping circuit theorem.	Remember	CAEC006.03
14	List the applications of Clamping Circuit	Remember	CAEC006.03
15	Draw the circuit diagram of Slicer.	Understand	CAEC006.02
PART-B (LONG ANSWER QUESTIONS)			
1	Explain the response of RC High Pass circuit for the square input, and draw the response with different time constants.	Understand	CAEC006.01
2	Explain the response of RC High Pass circuit for the pulse input, and draw the response with different time constants.	Understand	CAEC006.01
3	Prove that for any periodic input wave form the average level of the steady state output signal from an RC high pass circuit is always zero.	Understand	CAEC006.01
4	Compare the relationship between rise time, Bandwidth, and RC time constant of a low pass RC circuit.	Understand	CAEC006.01
5	Explain the response of RC Low Pass circuit for the square input, and draw the response with different time constants.	Understand	CAEC006.01
6	Explain the response of RC Low Pass circuit for the given step input waveforms.	Understand	CAEC006.01
7	Discuss the clamping circuit theorem.	Remember	CAEC006.03
8	List the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristics.	Remember	CAEC006.02
9	Explain positive peak clipping without reference voltage.	Understand	CAEC006.02

S. No	Questions	Blooms Taxonomy Level	Course learning Outcome
10	Explain about positive peak voltage limiters above reference level.	Understand	CAEC006.03
11	Draw the basic circuit diagram of positive clamper circuit and explain its operation.	Understand	CAEC006.03
12	Compare series diode clipper and shunt diode clipper.	Remember	CAEC006.02
13	Explain in brief about Practical Clamping.	Understand	CAEC006.03
14	Draw the diode shunt clipper that clips the sine wave signal above +5V and below -5V.	Understand	CAEC006.02
15	Explain the operation two level clipper with reference voltages, and sketch the output waveforms.	Understand	CAEC006.02
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)			
1	A pulse of 5 V amplitude and pulse width of 0.5m sec is applied to a high pass RC circuit consisting of R=22 K ohms and C= 0.47μF. Draw the output waveform and determine the percentage tilt in the output.	Understand	CAEC006.01
2	Draw the RC differentiator circuit for pulses of 1ms repletion and 10V amplitude. The trigger pulses are to have 8V amplitude. The source resistance is 50Ω and load resistance is 500Ω.	Understand	CAEC006.01
3	A 1KHz square wave output from an amplifier has rise time t_r = 250 ns and tilt = 10%, identify the upper and lower frequencies.	Understand	CAEC006.01
4	A 10Hz square wave is fed to an amplifier. Identify and sketch the output wave forms under following conditions. The lower 3db frequency is i) 0.3Hz ii) 3Hz iii) 30Hz	Understand	CAEC006.01
5	A symmetrical square wave whose peak-to-peak amplitude is 2V and whose average value is zero is applied to on RC integrating circuit. The time constant is equals to half -period of the square wave. Identify the peak to peak value of the output amplitude.	Understand	CAEC006.01
6	A 100V peak square wave with an average value of 0V and a period of 20 ms is to be negatively clamped at 25V. Draw the input and output waveforms.	Understand	CAEC006.03
7	Identify the value of Resistance R in clipper circuit when forward Resistance of diode is 10k Ω and reverse resistance of diode is 100k Ω.	Understand	CAEC006.02
8	For the clipper circuit shown in figure, the input vi = vi = 60 sin ωt. Observe and plot to Scale i) The transfer characteristic indicating slopes and intercepts. Ii) Input / output on the same scale. Assume ideal diodes. 	Understand	CAEC006.02
9	Draw the diode clamper circuit to clamp the positive peaks of the input signal at zero level. The frequency of the input signal is 500 Hz.	Understand	CAEC006.03
10	A 100V peak square wave with an average value of 0V is to be negatively Clamped at 25V. Draw the output waveforms.	Understand	CAEC006.03
UNIT-II			
MULTIVIBRATORS			
PART-A(SHORT ANSWER QUESTIONS)			
1	Define Multivibrator. List out the different types of Multivibrator.	Remember	CAEC006.04
2	Distinguish between Stable state and a Quasi Stable state in a Multivibrator.	Understand	CAEC006.04

S. No	Questions	Blooms Taxonomy Level	Course learning Outcome
3	List the other names for describing the Bistable Multivibrator.	Remember	CAEC006.04
4	Define Settling time, transition time in a Bistable Multivibrator.	Remember	CAEC006.04
5	Show that the resolving time is the sum of the transition time and the settling time.	Understand	CAEC006.04
6	Discuss the different methods of Triggering.	Understand	CAEC006.04
7	Explain the role of Commutating Capacitors.	Understand	CAEC006.04
8	List the Expression for Maximum frequency of Bistable Multivibrator.	Remember	CAEC006.04
9	List the other names for the Monostable Multivibrator.	Remember	CAEC006.06
10	Name any two methods to eliminate the Hysteresis in Schmitt Trigger.	Remember	CAEC006.05
11	List the expression of pulse width of Monostable Multivibrator.	Remember	CAEC006.06
12	Define terms UTP and LTP.	Remember	CAEC006.05
13	List the expression of frequency of Oscillations in Astable Multivibrator.	Remember	CAEC006.06
14	Show that an Astable Multivibrator is also called square Wave generator.	Understand	CAEC006.06
15	Explain monostable acts as voltage to time converter.		
PART-B (LONG ANSWER QUESTIONS)			
1	Explain the operation of bistable multivibrator circuit with circuit diagram and waveform.	Understand	CAEC006.04
2	Explain with the help of neat circuit diagram the principle of operation of monostable multivibrator, and derive an expression for pulse width.	Understand	CAEC006.06
3	Discuss the operation of Astable multi vibrator using circuit diagram.	Understand	CAEC006.06
4	Explain the operation of monostable multivibrator using circuit diagram.	Understand	CAEC006.06
5	Discuss the triggering methods for multivibrattors.	Understand	CAEC006.04
6	Explain the working of a Self bias Bistable multivibrator circuit with the help of waveforms and circuit diagram.	Understand	CAEC006.04
7	Find the expression for gate width of a Monostable Multivibrator neglecting the reverse saturation current I_{CBO}.	Understand	CAEC006.06
8	Explain the working of a collector coupled Astable Multivibrator. Obtain the expression for frequency in Astable Multivibrator With the help of neat circuit diagram and waveforms.	Understand	CAEC006.06
9	Discuss the operation of Schmitt trigger with UTP and LTP.	Understand	CAEC006.05
10	Derive the expressions for triggering points for Schmitt trigger.	Understand	CAEC006.05
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)			
1	Design a Schmitt trigger circuit using NPN transistors having h_{FE}(MIN) =60 . VBE cut-off = 0V, V_{CE}(Sat) = 0.2V and VBE(Sat) = 0.7V. Given Vcc=8V and o/p swing = 6V, UTP = 3.5V, LTP = 1.5V, R1 = 10K Ω & R2 = 2K Ω. Determine Rc1, Rc2 and Re.	Understand	CAEC006.05
2	A collector coupled Fixed bias binary uses NPN transistors with hFE = 100. The circuit parameters are VCC = 12v, VBB = -3v,RC = 1k Ω , R1 = 5k Ω , and R2 = 10 k Ω . Verify that when one transistor is cut-off the other is in saturation. Find the stable state currents and voltages for the circuit. Assume for transistors VCE(sat) = 0.3V and VBE(sat) = 0.7V.	Understand	CAEC006.04
3	Design a Schmitt trigger circuit using n-p-n silicon transistors to meet the following specifications: Vcc=12v, UTP=4v, LTP=2v,hfe=60, Ic2=3mA. Use relevant assumptions and the empirical relationships.	Understand	CAEC006.05
4	Design a collector coupled astable multivibrator to meet the following Specifications: f =10KH Z,VCC =12V,I C (sat)=4mAand hFE (min)=20.Assume that V CE (sat)=0.3V and V BE (sat)=0.7V.	Remember	CAEC006.06
5	Design an astable multivibrator to generate 5kHz square wave with a duty cycle of 40% and if amplitude 12V. Use NPN transistor having hFE = 100, VBesat = 0.7V , VCEsat = 0.2, ICmax = 100mA. Show the waveforms seen at both the collector and bases.	Remember	CAEC006.06

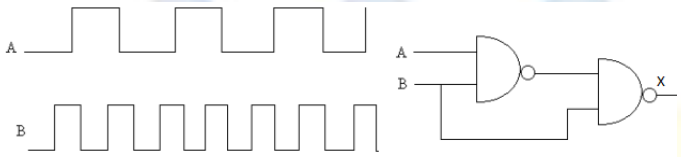
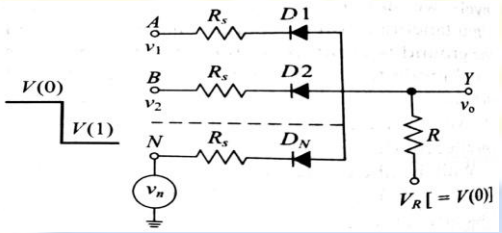
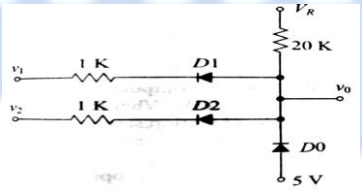
S. No	Questions	Blooms Taxonomy Level	Course learning Outcome
6	Silicon transistors with hfe = 30 are available. If Vcc = 12V and VBB= 6V, design a fixed bias bistable multivibrator.	Understand	CAEC006.04
7	Consider the Schmitt trigger with germanium transistor having hfe= 20. The circuit parameter ar e Vcc = 15V, Rs = 2kΩ, Rc1= 4kΩ, R1= 1 kΩ= 3 kΩ R2 = 10 kΩ and Re= 6 kΩ.Find LTP and UTP.	Understand	CAEC006.05
8	Design an astable multivibrator to generate a 5kHz square wave with a duty cycle of 60% and amplitude 12v. Use NPN silicon transistors having hFE(min)= 70, VCE(sat) = 0.3v, VBE(sat) = 0.7v, VBE(cutoff) = 0v and RC = 2K. Draw the waveforms seen at both collectors and bases.	Understand	CAEC006.06
9	Design a Fixed Bias binary by given fallowing specifications, Vcc=Vbb=12V, hfe(min) = 20, Ic(sat)=4mA Assume npn si-Transistors	Understand	CAEC006.04
10	Design Self Bias binary using si transistors. Vcc=6V, hfe(min) =30,Assume appropriate junction voltages for your design.	Understand	CAEC006.04
UNIT-III			
SAMPLING GATES AND TIME BASE GENERATORS			
PART-A(SHORT ANSWER QUESTIONS)			
1	Define Sampling gate.	Remember	CAEC006.07
2	Describe other names for sampling gate.	Understand	CAEC006.07
3	Compare the difference between sampling gate & logic gate.	Understand	CAEC006.07
4	Discuss different types of sampling gates.	Understand	CAEC006.07
5	Define Uni directional sampling gate.	Remember	CAEC006.07
6	Define Bi directional sampling gate.	Remember	CAEC006.07
7	Define gating signal.	Remember	CAEC006.07
8	Discuss the other names of gating signal.	Understand	CAEC006.07
9	List the applications of sampling gates.	Remember	CAEC006.07
10	List the drawbacks of Two- diode sampling gate.	Remember	CAEC006.07
11	Define pedestal of sampling gate.	Remember	CAEC006.07
12	Compare two diode and four diode sampling gate.	Remember	CAEC006.07
13	Show the circuit for uni directional sampling gate.	Understand	CAEC006.07
14	Discuss the advantage of shunt over series switch.	Understand	CAEC006.07
15	How to overcome pedestal in uni directional sampling gates.	Understand	CAEC006.07
SYLLABUS FOR CIE II			
1	Define sweep waveform.	Remember	CAEC006.08
2	Compare the voltage and current time base generator.	Understand	CAEC006.08
3	Which amplifier is used in miller time base generator?	Understand	CAEC006.08
4	Name the types of time base generators.	Remember	CAEC006.08
5	List the applications of time base generators.	Remember	CAEC006.08
6	Write the expression for sweep time of a UJT sweep circuit.	Understand	CAEC006.08
7	Write the expression for the slope error of miller and bootstrap time base generators.	Understand	CAEC006.08
8	Define slope error of sweep circuit.	Remember	CAEC006.08
9	Define displacement error of sweep circuit.	Remember	CAEC006.08
10	Define flyback time of sweep circuit.	Remember	CAEC006.08
11	Define transmission error of sweep circuit.	Remember	CAEC006.08
12	Express the sweep time of UJT.	Remember	CAEC006.08
13	Express the restoration time of UJT.	Remember	CAEC006.08
14	Draw the equivalent circuit of UJT.	Understand	CAEC006.08
15	Write the expression for e_s, e_d and e_t for an exponential sweep circuit.	Understand	CAEC006.08
PART-B(LONG ANSWER QUESTIONS)			
1	Explain the operation of Four diode bidirectional Sampling gate with neat sketch.	Remember	CAEC006.07

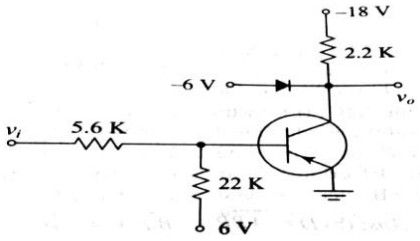
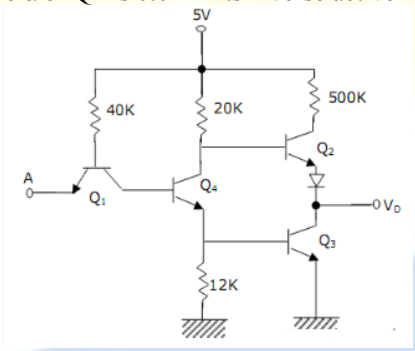
S. No	Questions	Blooms Taxonomy Level	Course learning Outcome
2	Find the expressions for gain and minimum control voltages of a bidirectional two- diode sampling gate.	Understand	CAEC006.07
3	Illustrate with neat circuit diagram, the operation of unidirectional sampling gate for multiple inputs.	Remember	CAEC006.07
4	Discuss the operation of unidirectional sampling gate with different control voltages.	Remember	CAEC006.07
5	Explain the basic operating principles of sampling gates	Remember	CAEC006.07
6	Explain the basic principles of sampling gates using series switch and also give the applications of sampling gate.	Understand	CAEC006.09
7	Discuss the operation of bidirectional sampling gate using transistor.	Remember	CAEC006.07
8	Explain the operation of unidirectional sampling gate for multiple gate signals.	Understand	CAEC006.07
9	Design the circuit of four-diode sampling gate. Derive expressions for its gain and Vmin.	Understand	CAEC006.07
10	Explain the effect of control voltage on gate output of unidirectional sampling gate using diode with some example.	Understand	CAEC006.07
SYLLABUS FOR CIE II			
1	Explain the methods to generate voltage time base waveform for different sweep circuits.	Remember	CAEC006.08
2	Explain the basic principles of Miller and Bootstrap time base generators.	Understand	CAEC006.08
3	Derive the terms slope error, displacement error of time-base signal.	Remember	CAEC006.08
4	Explain the working of a transistor Miller time base generator. With the help of neat circuit diagram and waveforms.	Understand	CAEC006.08
5	Design and clearly indicate the restoration time and fly back time on the typical waveform of a time base voltage. Solve the relation between the slope, transmission and displacement errors.	Remember	CAEC006.08
6	Define and derive transmission error pertaining to exponential sweep circuits with neat wave forms.	Remember	CAEC006.08
7	Explain the working of transistor Bootstrap time base generator with the help of neat diagram.	Understand	CAEC006.08
8	With the help of neat circuit diagram, explain the working of UJT sweep circuit.	Understand	CAEC006.08
9	Explain the transistor Miller time base generator with the help of circuit diagram.	Understand	CAEC006.08
10	Show the relationship between the sweep error, displacement error, and transmission error related to sweep circuits.	Understand	CAEC006.08
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)			
1	Assume Vs = 20V, Rf = 25Ω, $R_L = R_C$ = 100KΩ. Find, i. Gain (A) ii. Minimum positive control voltage (VCP)min iii. Minimum negative control voltage (Vcn) min for four diode sampling gate.	Understand	CAEC006.07
2	Design a transistor shunt gate to sample a signal current having peak amplitude of 2mA. Also calculate the output errors due to $V_{CE(sat)}$ and I_{CO}	Understand	CAEC006.07
3	Assume Vs = 40V, Rf = 25Ω, RL = Rc = 150KΩ. Find i) Gain (A) ii) Minimum positive control voltage (VCP)min iii) Minimum negative control voltage $(Vcn)_{min}$ for two diode sampling gate.	Understand	CAEC006.07
4	Design a transistor series gate to sample a signal with a peak amplitude 4v, and a source resistance of 200Ω.Also calculate the output errors due to $V_{CE(sat)}$ and I_{CO}.	Understand	CAEC006.07
SYLLABUS FOR CIE II			
1	Design a transistor bootstrap ramp generator to provide output amplitude	Understand	CAEC006.08

S. No	Questions	Blooms Taxonomy Level	Course learning Outcome
	of 12V over a time period of 2ms. The input signal is a negative going pulse with amplitude of 5 V, a pulse width of 2ms and the time interval between pulses is 0.5ms. The load resistance is 1K and the ramp is to be linear within 1%. The supply is to be 15V. Take hfe(min) = 80.		
2	In the UJT sweep circuit, V_{BB} = 20V, V_{yy} = 50V, R=5k, C=0.01μF, UJT has η= 0.5.Find i. amplitude of sweep signal ii. Slope and displacement errors and iii. Estimated recovery time.	Understand	CAEC006.08
3	A transistor bootstrap ramp generator is to produce a 15V, 5ms output to a 2kΩ load resistor. The ramp is to be linear within2%. Design a suitable circuit using V_{cc} = 22V, $-V_{EE}$ = -22V and transistor with $h_{fe(min)}$ = 25. The input pulse has an amplitude of -5V, pulse width = 5ms , space width = 2.5 ms.	Remember	CAEC006.08
4	Calculate sweep interval of a UJT sweep circuit for following specifications. η = 0.68, V_{BB} = 12V, Vv = 0.8V, Vp = 6V.	Understand	CAEC006.08
5	The transistorized Bootstrap sweep generator circuit has the following parameters: VCC = 25V, -VEE = -15V, R = 10 KΩ, RB = 150 KΩ, RE= 1KΩ, C = 0.05 μF. The gating waveform has 300μs duration. The transistor parameters are hie = 1.1KΩ, hre = 2.5 x 10-4, hfe =50, hoe = 25μA/V. a. Draw the waveforms for the collector current of input transistor (Q1), IC1 and output voltage at the emitter of output transistor (Q2), labeling all current and voltage levels. b. What is the slope error of the sweep? c. What is the sweep speed and the maximum value of the sweep voltage. d. What is the retrace time Tr for C to discharge completely. e. Calculate the recovery time T1 for C1 to recharge completely.	Understand	CAEC006.08
UNIT-IV			
SYNCHRONIZATION AND FREQUENCY DIVISION			
PART-A (SHORT ANSWER QUESTIONS)			
1	Define Relaxation circuit. Give Some examples.	Remember	CAEC006.10
2	Define Synchronization.	Remember	CAEC006.10
3	Name some negative resistance devices used as relaxation Oscillator.	Remember	CAEC006.10
4	Define the terms Sweep time and Restoration time.	Remember	CAEC006.10
5	Define phase delay.	Remember	CAEC006.11
6	Distinguish between Synchronization and synchronization with frequency division.	Understand	CAEC006.10
7	Compare Sine wave synchronization with pulse synchronization.	Understand	CAEC006.10
8	Illustrate the condition to be met for pulse synchronization.	Understand	CAEC006.10
9	Why does phase delay occur.	Understand	CAEC006.11
10	Define phase jitter.	Remember	CAEC006.11
11	List the different types of Synchronization.	Remember	CAEC006.10
12	Indicate the condition for frequency divider circuit.	Understand	CAEC006.11
13	Explain one to one basis system in frequency synchronization.	Remember	CAEC006.11
14	Compare phase delay and phase jitter.	Remember	CAEC006.10
15	Sketch the UJT relaxation circuit.	Understand	CAEC006.11
PART-B (LONG ANSWER QUESTIONS)			
1	Obtain pulse synchronization using UJT sweep circuit with help of circuit diagram and waveforms.	Understand	CAEC006.10
2	Explain sine wave frequency division using a sweep circuit with the help of neat waveforms	Understand	CAEC006.10
3	Discuss the principle of synchronization and synchronization with	Understand	CAEC006.10

S. No	Questions	Blooms Taxonomy Level	Course learning Outcome
	frequency division.		
4	Illustrate the method of pulse synchronization of relaxation devices, with examples.	Remember	CAEC006.12
5	Explain the frequency division in monostable multivibrator with the help of circuit diagram & waveforms.	Understand	CAEC006.11
6	Define the terms phase delay and phase jitter. What is the condition to be met for pulse synchronization.	Remember	CAEC006.11
7	Explain the use of a monostable relaxation device as a divider.	Understand	CAEC006.11
8	How does the synch signal affect the frequency of operation of the sweep generator.	Understand	CAEC006.11
9	Obtain the frequency division of an Astable multivibrator using pulse signals With the help of a circuit diagram and waveforms.	Understand	CAEC006.11
10	Explain the synchronization of a sweep circuit with symmetrical signals.	Understand	CAEC006.12
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)			
1	Design a relaxation oscillator to have 3khz output frequency. Using UJT and a 20v supply, Calculate the sweep amplitude. The specifications from the data sheet are given as η=0.7, Ip=2_A, Iv=1nA and V_{EBSAT}=3V.	Understand	CAEC006.10
2	The relaxation oscillator, when running freely, generates an output signal of peak - to - peak amplitude 100V and frequency 1 kHz. Synchronizing pulses are applied of such amplitude that at each pulse the breakdown voltage is lowered by 20V. Over what frequency range may the sync pulse frequency be varied if 1 : 1 synchronization is to result? If 5 : 1 synchronization is to be obtained (fP /fS = 5), over what range of frequency may the pulse source be varied?	Understand	CAEC006.10
3	The relaxation oscillator when running freely generates output sweep amplitude of 100V and frequency 1kHz. Synchronizing pulses are applied such that at each pulse the breakdown voltage is lowered by 20V. Over what frequency range the synchronizing pulse frequency may be varied if 1:1 synchronization is to result.	Understand	CAEC006.10
4	A symmetrical Astable multivibrator using germanium transistors and operating from a 10V collector supply voltage has a free period of 1000 µsec. Triggering pulses whose spacing is 750 µsec are applied to one base through a small capacitor from a high impedance source. Find the minimum triggering pulse amplitude required to achieve 1: 1 synchronization. Assume typical junction voltage of the transistor and that the timing portion of the base waveform is linear.	Understand	CAEC006.11
5	A UJT sweep operates with Vv = 3V, Vp=16V and η=0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronism with the sync signal.	Remember	CAEC006.11
6	A UJT is used as a switch across a sweep capacitor C which charges through R. A single voltage supply V_{BB} is used in the circuit. If V_V&V_P are the valley and peak voltages respectively, Prove that the sweep duration is exactly given by Ts = RC ln (V_{BB} – V_V)/(V_{BB} –V_P).	Understand	CAEC006.10
7	Frequency division of 6:1 is obtained with an Astable multivibrator, negative pulses are applied simultaneously to both bases of the n-p-n transistors. The OFF time of $Q_1(V_1)$ is twice that of $Q_2(V_2)$. Sketch the wave shapes at Base terminals.	Remember	CAEC006.12
8	A symmetrical Astable multivibrator is synchronized with pulses from a high-impedance source applied to one base. Draw a diagram and Show the range of synchronization as a function of the pulse amplitude and frequency.	Remember	CAEC006.12

S. No	Questions	Blooms Taxonomy Level	Course learning Outcome
9	Pulses from a high-impedance source are applied through a small capacitance to one base of a symmetrical Astable multi. Show that if $1.5T_0<T_p<2T_0$, then the multi waveform will consist of alternate cycles which are not alike. Show that the same result is obtained if a multi is considered.	Understand	CAEC006.12
10	A symmetrical Astable multivibrator using germanium transistors and operating from a 12V collector supply voltage has a free period of 500Hz. Pulses of 0.5V amplitude from a high-impedance source are applied to one base. Assume that the timing portion of the base waveform is linear. (a) if 1:1 synch is to be obtained, over what range may the pulse frequency be varied.	Remember	CAEC006.12
UNIT-V			
DIGITAL LOGIC FAMILIES			
PART-A(SHORT ANSWER QUESTIONS)			
1	Discuss the classification of logic families.	Understand	CAEC006.13
2	What are the classifications of saturated bipolar logic families.	Understand	CAEC006.13
3	Define Fan-out of a logic family.	Understand	CAEC006.14
4	Define Fan-in of a logic family.	Understand	CAEC006.14
5	Define power dissipation of a logic family.	Understand	CAEC006.14
6	Define noise margin of a logic family.	Understand	CAEC006.14
7	Name the three types of TTL gate.	Remember	CAEC006.14
8	Sketch the RTL OR gate.	Remember	CAEC006.15
9	List out the advantages and disadvantages of totem pole configuration.	Understand	CAEC006.14
10	Compare merits and demerits of ECL.	Remember	CAEC006.14
11	Discuss any two characteristics of ECL gates.	Understand	CAEC006.14
12	Identify the logic family for simple and Most complex fabrication.	Understand	CAEC006.14
13	Design the circuit diagram of diode resistor logic AND gate.	Remember	CAEC006.15
14	Draw the Totem-pole configuration of TTL gate.	Remember	CAEC006.14
15	Construct CMOS NAND gate.	Remember	CAEC006.15
PART-B (LONG ANSWER QUESTIONS)			
1	Discuss the two input OR gate using RTL Logic and explain its operation with truth table.	Remember	CAEC006.15
2	Compare the different logic family's related different parameters.	Remember	CAEC006.14
3	Explain the operation of TTL NAND gate with circuit diagram.	Understand	CAEC006.15
4	Construct a three input AND gate and verify its truth table using diodes & Resistors.	Apply	CAEC006.15
5	Explain the working of transistor Inverter logic using circuit diagram and show its truth table.	Understand	CAEC006.15
6	Explain the operation of diode - resistor logic AND & OR gate using circuit diagram	Understand	CAEC006.15
7	Realize a three- input NAND gate using Transistor -Transistor Logic. Explain its operation with Totem- pole.	Understand	CAEC006.15
8	Describe the operation of emitter coupled logic with its advantages and disadvantages.	Remember	CAEC006.15
9	Define the terms of the following, i. Wired-AND connection ii. Current Source-sink Logic iii. Tristate Logic	Understand	CAEC006.15
10	Describe Logical noise in a diode AND gate. Explain how it can be reduced by connecting a clamping diode in the circuit.	Remember	CAEC006.15
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)			
1	Design a transistor inverter circuit (NOT gate) with the following	Remember	CAEC006.13

S. No	Questions	Blooms Taxonomy Level	Course learning Outcome
	specifications: $V_{CC} = V_{BB} = 10V$, $I_{Csat} = 10mA$, hfe(min) = 30. The input is varying between 0 and 10V. Assume typical junction voltages of npn silicon transistor		
2	The transistor inverter (NOT gate) circuit has hfe(min) = 40, V_{cc} = 12V, R_c =2.2kΩ, R1 = 15k Ω and R2 = 100k Ω, V_{BB} = 12V. The input is varying between 12 V and 0V. Assume typical junction voltages of pnp transistor. How this circuit works as NOT gate.	Understand	CAEC006.13
3	Draw the output waveform X for the given inputs for below figure. 	Understand	CAEC006.13
4	Consider two signals, a 1KHz sine wave and a 10KHz square-wave of zero average value, applied to the OR circuit of fig. with Vr=0. Draw the output waveform if the sine-wave amplitude a) exceeds the square wave amplitude, b) is less than the square wave amplitude. 	Understand	CAEC006.13
5	The binary input levels for the AND circuit shown are V(0)=0V and V(1)=25V.Assume ideal diodes. If V1= V(0) and V2=V(1), then v0 is to be at 5V.However, if v1=v2=V(1), then v0 is to rise above 5V.(a) what is the max value of VR which may be used (b) if V_R=20V, what is V_0, at a coincidence[V1=V2=V(1)]. 	Understand	CAEC006.13
6	Find v0 and v if (a) there are no pulses at either A or B (b) there is a 30V positive pulse at A or B and (c) there are positive pulses at both A and B.(d)What is the min pulse amplitude which must be applied in order that the circuit operate properly. Assume ideal diodes.	Understand	CAEC006.14
7	The two-input diode AND circuit shown uses diodes with Rf=500 Ω, Rr=∞ and the currents in D1 and D2 are each 4 mA. Then Calculate the quiescent output voltage v0 and the values of R and R'.	Remember	CAEC006.14
8	Verify that the circuit shown is an inverter by calculating the output levels corresponding to input levels of 0 and -6V.What min value of h_{FE} is required. Neglect junction saturation voltages and assume an ideal diode.	Remember	CAEC006.14

S. No	Questions	Blooms Taxonomy Level	Course learning Outcome
			
9	The two-input diode AND circuit shown uses diodes with R_f= 200Ω, R_r= 1M Ω and the currents in D1 and D2 are each 2 mA & 6mA respectively. Then Calculate the output voltage when one input diode is cut-off.	Remember	CAEC006.15
10	For TTL circuit shown below find the current flowing through the collector of transistor Q4 when V0 = 0.2V, assume V_{CEsat} = 0.2 V, β= 100 & V_{BEsat} = 0.7V. the α of Q1 is 0.01 in its inverse active mode. 	Understand	CAEC006.15

HOD, ECE.