INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Name	:	**FPGA ARCHITECTURES AND APPLICATIONS**
Course Code	:	**BES005**
Class	:	**I M. Tech**
Branch	:	**EMBEDDED SYSTEMS**
Academic Year	:	**2017– 2018**
Course Faculty	:	**Dr. V. Vijay, Professor**

COURSE OBJECTIVES:

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

TUTORIAL QUESTION BANK

S. No	QUESTION	Blooms Taxonomy Level	Course learning Outcome
UNIT-I			
Group – A (Short Answer Questions)			
1	What is meant by programmable array logic?	Understand	1
2	What is meant by programmable logic array?	Analyze	1
3	What is meant by generic array logic?	Analyze	1
4	List the types of read only memories.	Understand	1
5	What is meant by parallel adder?	Understand	1
6	Explain the functional blocks of CPLD.	Understand	1
7	Draw a PROM cell.	Apply	1
8	Draw a block diagram of PAL.	Apply	1
9	Draw a block diagram of PLA.	Understand	1
10	Draw a block diagram of GAL.	Understand	1
Group – B (Long Answer Questions)			
1	Distinguish between ROM , PLA and PAL.	Apply	2
2	Describe the architecture of XCR3064XL CPLD.	Apply	3
3	Compare EEPROM and FLASH memory technology.	Apply	3
4	Design of combinational logic circuits using PLA,PAL and GAL	Apply	3
5	Design of sequential logic circuits using PLA,PAL and GAL	Understand	3
6	Design of full adder using PAL and PLA.	Create	3

S. No	QUESTION	Blooms Taxonomy Level	Course learning Outcome
7	Design of counter using PAL and PLA.	Apply	3
8	Design of adder with accumulation using CPLD.	Apply	3
9	Draw and explain the functional blocks of CPGA architecture.	Apply	3
10	List the features of complex programmable logic device.	Apply	3
UNIT-II			
Group – A (Short Answer Questions)			
1	What are the types of FPGA?	Understand	3
2	Draw the architecture of CLB.	Understand	4
3	What are the features of FPGAS.	Apply	4
4	Write about programmable interconnects in FPGAs.	Understand	4
5	List out the advantages of FPGA.	Apply	4
6	Write about dedicated specialized components of FPGA.	Remember	4
7	What are the limitations of FPGA.	Understand	4
8	Write the applications of FPGAs.	Remember	4
Group – B (Long Answer Questions)			
1	How granularity of logic block influences the performance of an FPGA	Remember	4
2	Give the routing architectures and logic Blocks of FPGA.	Understand	4
3	Explain about FPGA programming technologies.	Apply	4
4	Explain about programmable I/O blocks in FPGAs.	Remember	4
5	Describe about Programmable logic block architectures in FPGAs.	Understand	4
6	Describe the organization of FPGA.	Apply	4
7	Discuss about technology mapping for FPGAs.	Remember	4
8	Discuss about features of FPGAs.	Understand	4
UNIT-III			
Group – A (Short Answer Questions)			
1	Draw a four transistor RAM cell.	Understand	5
2	Draw a six transistor RAM cell.	Remember	5
3	List the advantages of SRAM based programming methods.	Apply	5
4	List the disadvantages of SRAM based programming methods.	Remember	5
5	Explain the CLB of Xilinx XC 4000 architecture.	Remember	5
6	Explain the I/O block of XC 4000 architecture.	Remember	5
7	Explain the I/O block of XC 4000 architecture.	Understand	5
8	Describe the function of Xilinx XC4000 logic block.	Understand	5
9	Describe the function of Xilinx XC3000 logic block.	Understand	5
10	Explain the operation of pass transistors in SRAM programming.	Remember	6
Group – B (Long Answer Questions)			
1	Describe the function of Xilinx XC2000 logic block.	Evaluate	7
2	Explain the functional blocks of Xilinx XC 2000 architecture.	Understand	7
3	Illustrate the switch matrix connection of Xilinx XC 2000 architecture	Apply	7
4	Explain the CLB of Xilinx XC 2000 architecture.	Analyze	7
5	Explain the I/O block of XC 2000 architecture.	Understand	7
6	Explain the operation of pass transistors and transmission gates in SRAM programming.	Analyze	7
7	Illustrate the role of look up tables in Xilinx XC series architectures.	Understand	7
8	Compare the architecture of Xilinx 2000 and Xilinx 3000 architecture.	Remember	7
9	Describe the function of Xilinx XC4000 logic block.	Understand	7
10	Explain the functional blocks of Xilinx XC 3000 architecture.	Remember	7
UNIT-IV			

S. No	QUESTION	Blooms Taxonomy Level	Course learning Outcome
Group – A (Short Answer Questions)			
1	Draw the Actel architecture in block level.	Understand	5
2	Describe the meaning of antifuse.	Remember	5
3	Explain about PLICE.	Apply	5
4	Draw the PLICE cross section view.	Understand	5
5	Draw the ACT2 architecture.	Understand	5
6	Explain ACT3 IO Module.	Remember	5
7	Draw the FPGA design flow.	Understand	5
8	Explain chip level considerations of ACT 1.	Understand	5
9	Give the differences between FPGA and PLDs.	Apply	5
10	Explain the Jitter Bounded PLL applications.	Understand	6
Group – B (Long Answer Questions)			
1	Discuss the concept of ACT 2 architecture	Evaluate	7
2	Relate Shannon expansion theorem in ACT architectures.	Understand	7
3	With neat diagram explain the functional blocks of ACT 3 architecture.	Apply	7
4	Describe the functionality of ACT 2 architecture	Analyze	7
5	Discuss the features of ACT 3 architecture.	Understand	7
6	Describe the functionality of ACT 1 architecture.	Analyze	7
UNIT-V			
Group – A (Short Answer Questions)			
1	Explaing the applications of ACT 1 and ACT 2.	Understand	7
2	Draw the ACTMAP Design flow.	Remember	7
3	Draw the ACT 1 five bit counter.	Apply	7
4	Draw the Act 2 Six-Bit Loadable Counter.	Understand	7
5	Explain the stpes involved in Pre-scaled Counter Design.	Understand	7
6	Explain about carry macro cell.	Remember	7
7	Explain S-module and draw the 16 bit accumulator.	Remember	7
8	Explain about state machine design.	Remember	8
9	Explain about pulse steal PLL.	Understand	8
10	Explain the features of fast DMA controller.	Understand	8
Group – B (Long Answer Questions)			
1	Design a counter using suitable programmable logic device.	Evaluate	8
2	Describe the operation of fast video controller for a robot manipulator.	Understand	8
3	Explain the operation of fast DMA controller.	Analyze	8
4	Design the accumulator using ACT architectures.	Understand	8
5	Design a synchronous counter using ACT devices.	Analyze	8
6	Discuss the concept of position tracker in robot manipulator.	Analyze	8
7	Mention the design issues of ACT architectures.	Understand	8
8	Design a adder using ACT architectures.	Analyze	8

HEAD OF THE DEPARTMENT,

ELECTRONICS AND COMMUNICATION ENGINEERING.