# INSTITUTE OF AERONAUTICAL ENGINEERING

**(Autonomous)**
Dundigal, Hyderabad - 500 043

## ELECTRICAL AND ELECTRONICS ENGINEERING

## TUTORIAL QUESTION BANK

| | | |
|---|---|---|
| **Course Name** | : | **DIGITAL AND PULSE CIRCUITS** |
| **Course Code** | : | **AEC019** |
| **Class** | : | **B. Tech IV Semester** |
| **Branch** | : | **EEE** |
| **Year** | : | **2018– 2019** |
| **Course Coordinator** | : | **Dr.V.Vijay Kumar, Assistant Professor, ECE** |
| **Course Faculty** | : | **MS.V.Bindusree, Assistant Professor, ECE** |

## COURSE OBJECTIVES:

**The course should enable the students to**

| S. NO | DESCRIPTION |
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| I | Understand basics, different binary codes in digital electronic circuits and be able to convert between different codes. |
| II | Implement minimization techniques and state machines using flip-flops. |
| III | Implement and design logical operations using large scale integration and medium scale integration devices. |
| IV | Discuss the concept of sequential circuits and analyze sequential systems. |
| V | Interpret the concept of feedback and classify various types of feedback amplifiers |
| VI | Understand the principle of oscillation and design different types of oscillators. |
| VII | Design and analyse single stage and multi stage Amplifiers |

## COURSE LEARNING OUTCOMES:

**Students, who complete the course, will have demonstrated the ability to do the following.**

| S.NO | DESCRIPTION |
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| CAEC019.01 | Understand number systems, binary addition and subtraction, 2's complement representation and operations with this representation and understand the different binary codes. |
| CAEC019.02 | Illustrate the switching algebra theorems and apply them for reduction of Boolean function. |
| CAEC019.03 | Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits. |
| CAEC019.04 | Discuss about digital logic gates and their properties, and implement logic gates using universal gates. |
| CAEC019.05 | Evaluate functions using various types of minimizing algorithms like Boolean algebra. |
| CAEC019.06 | Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method |
| CAEC019.07 | Design Gate level minimization using K-Maps and realize the Boolean function using logic gates. |
| CAEC019.08 | Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder. |
| CAEC019.09 | Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops. |
| CAEC019.10 | Analyze and apply the design procedures of small sequential circuits to build the gated latches. |
| CAEC019.11 | Understand the concept of Shift Registers and implement the bidirectional and universal shift registers. |

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| CAEC019.12 | Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops. |
| CAEC019.13 | Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops. |
| CAEC019.14 | Understand the design analysis of feedback amplifiers& types of feedback circuits |
| CAEC019.15 | Design various sinusoidal Oscillators like RC Phase shift, Wien bridge, Hartley and Colpitts oscillator for various frequency ranges |
| CAEC019.16 | Analyze the design of BJT as single stage and multistage amplifier circuits |
| CAEC019.17 | Implement the design analysis of coupling amplifiers and types of coupling circuits |

| S. No | QUESTION | Blooms Taxonomy Level | Course Learning Outcome |
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| **UNIT-I** | | | |
| **BOOLEAN ALGEBRA AND SWITCHING FUNCTIONS** | | | |
| **PART-A (SHORT ANSWER QUESTIONS)** | | | |
| 1 | Write short notes on binary number systems. | Remember | CAEC019.01 |
| 2 | Discuss 1's and 2's complement methods of subtraction. | Understand | CAEC019.01 |
| 3 | Discuss octal number system. | Understand | CAEC019.01 |
| 4 | Convert the octal numbers into binary numbers (47.5)8, (32.3)8. | Remember | CAEC019.01 |
| 5 | Show an example to convert gray code to binary code. | Understand | CAEC019.01 |
| 6 | Describe a short note on four bit BCD codes. | Remember | CAEC019.01 |
| 7 | Illustrate about unit–distance code? State where they are used. | Understand | CAEC019.01 |
| 8 | State error correcting codes. | Remember | CAEC019.01 |
| 9 | Convert 10101101.0111 to octal equivalent and hexadecimal equivalent. | Understand | CAEC019.01 |
| 10 | State about logic design and what do you mean by positive logic system. | Remember | CAEC019.01 |
| 11 | Identify Y for a given problem is (2.3)8 + (1.7)8 = (Y)8. | Understand | CAEC019.01 |
| 12 | Explain the specialty of unit –distance code. | Remember | CAEC019.01 |
| 13 | Convert (4065)8 into base 5. | Understand | CAEC019.01 |
| 14 | Convert (4065)8 into base 3. | Remember | CAEC019.01 |
| 15 | Convert $11001_2$ into decimal? | Remember | CAEC019.01 |
| **PART-B (LONG ANSWER QUESTIONS)** | | | |
| 1 | Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.<br>i. 100 – 110000 ii. 11010 - 1101. | Understand | CAEC019.01 |
| 2 | a) Rewrite the decimal number (215)10 as an octal number<br>b)Find (3250 - 72532)10 using 9's complement<br>c) Change (1001011101)2 to a hexadecimal number? | Remember | CAEC019.01 |
| 3 | a) Find (3250 - 72532)10 using 10's complement?<br>b) Convert (B3D9)16 to a binary number.<br>c) Convert (10110101)2 to decimal equivalent? | Understand | CAEC019.01 |
| 4 | a) Convert 4510 to binary number<br>b) Convert 0.62510 to binary number? | Remember | CAEC019.01 |
| 5 | (a) Add 01100100 by 00011001.<br>(b) Given that (292)10 = (1204)b determine `b'. | Understand | CAEC019.01 |
| 6 | (a) What is the gray code equivalent of the Hex Number 3A7.<br>(b) Find 9's complement of (25.639)10? | Remember | CAEC019.01 |
| 7 | (a) Find (72532 - 03250) using 9's complement.<br>(b) Express each number as an octal number. a.$101001001_2$ b. $1234_{16}$ | Understand | CAEC019.01 |
| 8 | Explain Self complemented codes. | Understand | CAEC019.01 |
| 9 | Convert (4085)10 into base-4 and obtain its 9's complement. | Remember | CAEC019.01 |
| 10 | Convert the following Hexadecimal number to their Decimal equivalent (EAF2)16. | Remember | CAEC019.01 |

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| **PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)** | | | |
| 1 | Given the 8bit data word 01011011, generate the 12-bit composite word for the hamming code that corrects and detects single errors. | Remember | CAEC019.01 |
| 2 | Express each number as an octal number. a. (101001001)2 b. (1001010000100010)2 c. (B78)16 d. (1234)16 | Understand | CAEC019.01 |
| 3 | A device transmits the binary data using even parity, the message is 1011001. Identify the receiver receives the correct data or not. | Remember | CAEC019.01 |
| 4 | Subtract the following binary numbers using 1's complement.<br>i) 1011-101 ii) 10110-1011 | Remember | CAEC019.01 |
| 5 | Differentiate between BCD code and 2421 code and XS-3. | Understand | CAEC019.01 |
| 6 | Find 7-bit hamming code for given message 1010 by using odd parity. | Understand | CAEC019.01 |
| 7 | The message below coded in the seven-bit hamming code is transmitted through a noisy channel. Decode the message assuming the at most a single error occurred in each code word.<br>1001011,0111001,1110110 | Remember | CAEC019.01 |
| 8 | Generate an 11-bit hamming code for a given data 1011010 using odd parity. | Remember | CAEC019.01 |
| 9 | Express each number as a hexadecimal number.<br>a. $(1010101010)_2$ b. $(2526)_8$ | Understand | CAEC019.01 |
| 10 | a. Convert $0.35_{10}$ to octal number.<br>b. Convert $9F2_{(16)}$ to its binary equivalent | Understand | CAEC019.01 |
| **UNIT-II** | | | |
| **MINIMIZATION TECHNIQUES AND DESIGN OF MSI** | | | |
| **PART-A (SHORT ANSWER QUESTIONS)** | | | |
| 1 | Define K-map. | Remember | CAEC019.06 |
| 2 | Define Implicant, Prime Implicant and Essential Prime Implicant. | Understand | CAEC019.06 |
| 3 | Define Consensus Theorem. | Remember | CAEC019.05 |
| 4 | Solve AB+BC+CA=AB+BC. | Remember | CAEC019.02 |
| 5 | Simplify the Boolean function A′BC +A′BC′ + AB′C′ + AB′C using K-map. | Understand | CAEC019.06 |
| 6 | Simplify the Boolean function x′yz + x′yz′ + xy′z′ + xy′z without using K-Map. | Understand | CAEC019.05 |
| 7 | Sketch and implement following logic function using k-map for given Y(A, B,C,D)= ∑m(0,1,2,3,4,7,8,9,10,11,12,14). | Remember | CAEC019.03 |
| 8 | Design a logic circuit to convert BCD and gray code. | Understand | CAEC019.08 |
| 9 | Design Full adder using Logic Gates. | Understand | CAEC019.08 |
| 10 | Design Half subtractor using NAND Gates. | Remember | CAEC019.08 |
| 11 | Design a Full adder using NAND Gates. | Understand | CAEC019.08 |
| 12 | Design a Full adder using NOR Gates. | Remember | CAEC019.08 |
| 13 | Design Half subtractor using NOR Gates. | Remember | CAEC019.08 |
| 14 | Design a Full subtractor using NAND Gates. | Understand | CAEC019.08 |
| 15 | Design a Full subtractor using NOR Gates. | Remember | CAEC019.08 |
| 16 | Design a full adder using two half adders. | Remember | CAEC019.08 |
| **PART-B (LONG ANSWER QUESTIONS)** | | | |
| 1 | Minimize the following function using K-map.<br>F (A, B, C, D) = ∑m (1, 3, 5, 7, 9, 10, 11, 12, 15). | Remember | CAEC019.06 |
| 2 | Minimize the following function using K-map f = ∑m (1, 2, 3, 5, 12, 13). | Remember | CAEC019.06 |
| 3 | Simplify the following Boolean expressions using K-map and implement them using logic gates. (a) F (A, B, C, D) = AB'C' + AC + A'CD'. (b) F (W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ. | Understand | CAEC019.05 |

| S. No | QUESTION | Blooms Taxonomy Level | Course Learning Outcome |
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| 4 | Minimize the following function using K-map.<br>F (A, B, C, D, E) = ∑m (1,3,5,7,9,10,11,12,15,19,21,22,27) + ∑d (0,4,8). | Understand | CAEC019.06 |
| 5 | Minimize the Boolean function F (w, x, y, z) = Σm (1, 3, 7, 11, 15) + Σd (0, 2, 5), obtain its POS Expression. | Remember | CAEC019.06 |
| 6 | Reduce the following expression using Karnaugh map (B 'A + A'B + AB'). | Understand | CAEC019.06 |
| 7 | Show that AB+AB'C+BC' = AC+BC'. | Remember | CAEC019.02 |
| 8 | Convert (A+B) (A+B+C)(B+C) Expression into canonical POS. | Understand | CAEC019.04 |
| 9 | Expand A (A'+B) (A'+B+C') to maxterms and minterms. | Remember | CAEC019.04 |
| 10 | Identify all the prime implicants and essential prime implicants for a given function using k-map. F (A, B, C, D) = Σm (0,1,2,5,6,7,8,9,10,13,14,15). | Remember | CAEC019.06 |
| **PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)** | | | |
| 1 | Implement the Boolean function F = AB + CD + E using NAND gates ? | Understand | CAEC019.04 |
| 2 | Simplify the Boolean function F (w, x, y, z) = Σm(1, 3, 7, 11, 15) + Σd (0, 2, 5). | Remember | CAEC019.06 |
| 3 | Design all logic gates using NAND. | Understand | CAEC019.04 |
| 4 | Design all logic gates using NOR. | Understand | CAEC019.04 |
| 5 | A function having three data inputs to implement the logic for the function F = Σm (0, 1, 2, 3, 4, 7). | Remember | CAEC019.06 |
| 6 | Construct and explain the working of decimal adder. | Understand | CAEC019.08 |
| 7 | Realize the Boolean expression for half subtractor. | Understand | CAEC019.08 |
| 8 | Simplify the Boolean function F = Σm (0, 1, 2, 3, 4, 7, 9, 10, 14, 15) using tabular method. | Understand | CAEC019.06 |
| 9 | Convert A.B.C+A.D expression into standard SOP form. | Understand | CAEC019.02 |
| 10 | Convert (A+B+C)(B+C')(A'+C) into standard POS form. | Understand | CAEC019.03 |
| **UNIT-III** | | | |
| **SEQUENTIAL CIRCUITS DESIGN** | | | |
| **PART-A (SHORT ANSWER QUESTIONS)** | | | |
| 1 | Define stable state? | Remember | CAEC019.09 |
| 2 | Define Flip-Flop? | Understand | CAEC019.09 |
| 3 | List the applications of Flip-Flops? | Remember | CAEC019.09 |
| 4 | Express your view about synchronous latch? | Understand | CAEC019.09 |
| 5 | How do you build a latch using universal gates? | Remember | CAEC019.09 |
| 6 | Explain about flip-flop memory characteristic? | Remember | CAEC019.09 |
| 7 | Distinguish between synchronous and asynchronous latch? | Understand | CAEC019.09 |
| 8 | Define clocked flip-flop? | Remember | CAEC019.09 |
| 9 | Why a gated D latch is called a transparent latch? | Understand | CAEC019.09 |
| 10 | List the two types of flip-flops? | Understand | CAEC019.09 |
| 11 | Explain about Different types of Latches in detail | Remember | CAEC019.09 |
| 12 | Explain about S-R (NOR gates) Latch? | Remember | CAEC019.09 |
| 13 | Explain about S-R (NAND gates) Latch? | Remember | CAEC019.09 |
| 14 | Draw The truth table of gated D-Latch? | | CAEC019.09 |
| 15 | Distinguish between Latch and Flip Flop? | Remember | CAEC019.09 |
| 16 | Draw The block diagram of sequential circuit? | Remember | CAEC019.09 |
| 17 | Determine the output state of S-R latch (active low) for S=1, R=0, Qn =1 | Understand | CAEC019.09 |
| 18 | Define Asynchronous sequential Circuit? | Remember | CAEC019.09 |
| 19 | Draw the gated S-R latch Logic Diagram? | Remember | CAEC019.09 |
| 20 | Determine the output state of S-R latch (active low) for S=0, R=0, Qn =1 | Understand | CAEC019.09 |
| 21 | Define binary cell? | Remember | CAEC019.09 |
| 22 | Draw The gated D-Latch logic diagram? | Remember | CAEC019.09 |

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| 23 | Determine the output state of gated D-latch for D=1, Qn = 0, enable=0. | Remember | CAEC019.09 |
| 24 | Draw the S-R Latch(NAND) Truth Table ? | Remember | CAEC019.09 |
| 25 | Why flip flops are edge triggered? | Remember | CAEC019.09 |
| | | | |
| 1 | List Shift registers? | Remember | CAEC019.12 |
| 2 | List the types of Shift registers. | Remember | CAEC019.12 |
| 3 | Explain basic difference between a shift register and counter? | Remember | CAEC019.11 |
| 4 | Classify the basic types of counters? | Understand | CAEC019.11 |
| 5 | Differentiate the advantages and disadvantages of ripple counters? | Remember | CAEC019.11 |
| 6 | Sketch mod 10 asynchronous counter? | Understand | CAEC019.11 |
| 7 | Sketch mod 6 asynchronous counter? | Understand | CAEC019.11 |
| 8 | How does a binary counter work? | Remember | CAEC019.09 |
| 9 | Sketch mod 5 asynchronous counter? | Remember | CAEC019.12 |
| 10 | State the use of clock pulse? | Remember | CAEC019.12 |
| 11 | Define race around condition? | Understand | CAEC019.12 |
| 12 | Explain function of the clock? | Understand | CAEC019.12 |
| 13 | Define level triggering? | Understand | CAEC019.12 |
| 14 | Draw the master-slave JK FF? | Remember | CAEC019.12 |
| 15 | Define synchronous counter? | Remember | CAEC019.12 |
| 16 | Define counter. | Remember | CAEC019.12 |
| 17 | Sketch MOD-6 counter? | Remember | CAEC019.12 |
| 18 | List the advantages of synchronous counters over asynchronous counters? | Remember | CAEC019.12 |
| 19 | Sketch Johnson counter using D-Flip Flop? | Remember | CAEC019.12 |
| 20 | Define Asynchronous counter? | Remember | CAEC019.12 |
| | **PART-B(LONG ANSWER QUESTIONS)** | | |
| 1 | Explain the working principle of JK Flip-Flop in detail. | Understand | CAEC019.09 |
| 2 | Define Latch. Explain about Different types of Latches in detail. | Remember | CAEC019.09 |
| 3 | Differentiate combinational and sequential circuits. | Understand | CAEC019.10 |
| 4 | Describe about T – Flip-flop with the help of a logic diagram and characteristic table. Derive a T-flip-flop from JK and D flip-flops. | Understand | CAEC019.09 |
| 5 | Explain with the help of a block diagram, the basic components of a Sequential Circuit? | Remember | CAEC019.12 |
| 6 | Explain about RS and JK flip-flops? | Remember | CAEC019.12 |
| 7 | Define T – Flip-flop with the help of a logic diagram and characteristic table? | Remember | CAEC019.12 |
| 8 | Define Latch. Explain about Different types of Latches in detail? | Remember | CAEC019.12 |
| 9 | Define JK – Flip-flop with the help of a logic diagram and characteristic table? | Remember | CAEC019.12 |
| 10 | List the characteristic equations for all Flip-Flops? | Remember | CAEC019.12 |
| | | | |
| 1 | Explain Serial Transfer in 4-bit shift Registers. | Remember | CAEC019.11 |
| 2 | Explain about Binary Ripple Counter. | Understand | CAEC019.13 |
| 3 | Explain the Ripple counter design. Also a decade counter design. | Remember | CAEC019.13 |
| 4 | Write short notes on shift register? Mention its applications. | Remember | CAEC019.11 |
| 5 | Design a left shift and right shift for the following data 10110101. | Understand | CAEC019.11 |
| 6 | Differentiate Synchronous and Asynchronous counters? | Remember | CAEC019.12 |
| 7 | Explain about Binary Ripple Counter? What is MOD counter? | Remember | CAEC019.12 |
| 8 | Define BCD Counter and Draw its State table for BCD Counter? | Remember | CAEC019.12 |

| S. No | QUESTION | Blooms Taxonomy Level | Course Learning Outcome |
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| 9 | Explain about Binary Ripple Counter? What is MOD counter? | Remember | CAEC019.12 |
| 10 | Explain the Ripple counter design. Also the decade counters design? | Remember | CAEC019.12 |
| **PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)** | | | |
| 1 | Convert a JK Flip Flop to i) SR Flip Flop ii) T Flip Flop iii) D Flip Flop | Understand | CAEC019.09 |
| 2 | Design mod 10 synchronous counter. | Remember | CAEC019.12 |
| 3 | Explain the operation of SR Flip-Flop using asynchronous inputs with truth table. | Remember | CAEC019.09 |
| 4 | Explain the Flip-Flop operating characteristics in detail | Remember | CAEC019.09 |
| 5 | Draw the schematic circuit of an edge triggered flip-flop with "active low preset" and "active low clear" using NAND gats and explain its operation. | Understand | CAEC019.09 |
| 6 | Give the transition table for the following flip-flops i) SR FF ii) D FF. | Understand | CAEC019.09 |
| 7 | Give the transition table for the following flip-flops i) JK FF ii) T FF. | Remember | CAEC019.09 |
| 8 | Explain the JK and Master slave Flipflop? Give its timing waveform? | Remember | CAEC019.12 |
| 9 | Explain the design of Synchronous Sequential circuit with an example? | Remember | CAEC019.09 |
| 10 | Write short notes on shift register? Mention its application along with the Serial Transfer in 4-bit shift Registers? | Remember | CAEC019.09 |
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| 1 | Design Johnson counter using JK flip flops. | Understand | CAEC019.12 |
| 2 | Design 3 bit asynchronous counter using SR flip flop. | Remember | CAEC019.13 |
| 3 | Design 4 bit synchronous counter using t flip flop. | Remember | CAEC019.12 |
| 4 | Design and implement 4-bit binary counter (using D flip flops) which counts all possible odd numbers only? | Remember | CAEC019.12 |
| 5 | Design a Ring counter using JK flipflop? | Remember | CAEC019.12 |
| 6 | Design MOD5 up and Down counter? | Remember | CAEC019.13 |
| 7 | Design a MOD-5 synchronous counter using flip flops and implement it? Also draw the timing diagram? | Remember | CAEC019.13 |
| 8 | Design a Twisted Ring counter using JK flipflop? | Remember | CAEC019.12 |
| 9 | Design a Modulo-12 up Synchronous counter using T-Flip Flops and draw the Circuit diagram. | Remember | CAEC019.09 |
| 10 | Design Johnson counters and state its advantages and disadvantages? | Remember | CAEC019.12 |
| **UNIT-IV** | | | |
| **FEEDBACK AMPLIFIERS AND OSCILLATORS** | | | |
| **PART-A (SHORT ANSWER QUESTIONS)** | | | |
| 1 | Define feedback and what are feedback amplifiers | Remember | CAEC019.14 |
| 2 | Define positive and negative feedback | Remember | CAEC019.15 |
| 3 | List the advantages and disadvantages of negative feedback | Understand | CAEC019.14 |
| 4 | Differentiate between voltage and current feedback in amplifiers | Understand | CAEC019.15 |
| 5 | Define Oscillator circuit | Understand | CAEC019.14 |
| 6 | List the classifications of Oscillators | Understand | CAEC019.15 |
| 7 | List the types of feedback oscillators | Understand | CAEC019.14 |
| 8 | State the frequency for RC phase shift oscillator | Remember | CAEC019.15 |
| 9 | Give the topology of current amplifier with current shunt feedback | Remember | CAEC019.14 |
| 10 | Define gain margin and phase margin | Remember | CAEC019.15 |
| 11 | Define LC oscillator | Remember | CAEC019.14 |
| 12 | Draw the circuit of Clapp oscillator | Remember | CAEC019.15 |
| 13 | How does an oscillator differ from an amplifier | Understand | CAEC019.14 |
| 14 | Define Barkhausen stability? | Remember | CAEC019.15 |
| 15 | Name two low frequency oscillators | Remember | CAEC019.14 |

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| **PART-B (LONG ANSWER QUESTIONS)** | | | |
| 1 | Explain the concept of feedback as applied to electronic amplifier circuits. What are the advantages and disadvantages of positive and negative feedback | Understand | CAEC019.14 |
| 2 | Explain the concept of feedback as applied to electronic amplifier circuits. What are the advantages and disadvantages of positive and negative feedback | Understand | CAEC019.15 |
| 3 | Explain the basic principle of generation of oscillations in LC tank circuits. What are the considerations to be made in the case of practical L.C. Oscillator Circuits? | Understand | CAEC019.14 |
| 4 | Draw the circuit for Voltage series amplifier and justify the type of feedback. | Remember | CAEC019.15 |
| 5 | Draw the circuit and explain the principle of operation of RC phase-shift oscillator circuit. What is the frequency range of generation of oscillations? Derive the expression for the frequency of oscillations. | Remember | CAEC019.14 |
| 6 | Draw the circuit for Current series amplifier and justify the type of feedback. Derive the expressions for Av, Ri and Ro for the circuit. | Remember | CAEC019.15 |
| 7 | Deduce the Barkausen Criterion for the generation of sustained oscillations. How are the oscillations initiated? | Understand | CAEC019.14 |
| 8 | Derive the expression for the frequency of Wein Bridge Oscillators. | Understand | CAEC019.15 |
| 9 | Draw the circuit for Voltage shunt amplifier and justify the type of feedback. Derive the expressions for Av, Ri and Ro for the circuit. | Understand | CAEC019.14 |
| 10 | Reason out the need for three identical R-C sections in R-C phase-shift oscillator circuits? | Understand | CAEC019.15 |
| **PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)** | | | |
| 1 | An amplifier has a voltage gain of 400, f150hz, f2=200KHz, and a distortion of 10% without feedback. Determine the amplifier voltage gain f1f, f2f and pf when a -ve feedback is applied with feedbak ration of 0.01? | Understand | CAEC019.15 |
| 2 | An amplifier has a mid band gain of 125 and bandwidth of 250 kHz. If 4% negative feedback is introduced, find the new bandwidth and gain. | Understand | CAEC019.15 |
| 3 | For a current series feedback amplifier Rs=1K, gmf=-2mA/V. Avf=-8 D=60 hfe=300. Find Re RL Rif Ic Q at room temperature | Remember | CAEC019.14 |
| 4 | An amplifier with Av = - 500, produces 5% harmonic distortion at full output. What value of β is required to reduce the distortion to 0.1 % ? What is the overall gain? | Remember | CAEC019.15 |
| 5 | 'For a voltage series feedback amplifier Find D, $A_{vf}$, $R_{if}$, $R_{of}$ . | Remember | CAEC019.14 |
| 6 | For a voltage shunt feedback amplifier Rs=8K,Rc=3K, RB=30K,. Find D, Avf, Rif, R', Rmf. hie=1K,hre=0,hfe=50,hoe=0. | Understand | CAEC019.14 |

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| 7 | A voltage-series -ve feedback amplifier has a voltage gain without feedback of A=500, $R_i$=3KΩ, Ro=20KΩ and feedback ratio β=0.01.Calculate the voltage gain $A_f$, $R_{if}$ and output resistance $R_{of}$ of amplifier with feedback? | Understand | CAEC019.15 |
| 8 | A Hartley oscillator is designed with L = 20μH and a variable capacitance. Find the Range of capacitance values if the frequency of oscillation is varied between 950 KHz to 2050 KHz. | Understand | CAEC019.16 |
| 9 | Find the capacitor C and hfe for the transistor to provide a resonating frequency of 10KHZ of a phase-shift oscillator. Assume R1=25k, R2=60k,Rc=40k, R=7.1k and hie=1.8k? | Remember | CAEC019.16 |
| 10 | A crystal has L=0.1H, C=0.01PF, R=10k and CM=1PF. Find the series resonance and Q-factor? | Remember | CAEC019.16 |
| **UNIT-V** | | | |
| **SINGLE STAGE AMPLIFIERS AND MULTI STAGE AMPLIFIERS** | | | |
| **PART-A(SHORT ANSWER QUESTIONS)** | | | |
| 1 | List the classification of amplifiers. | Remember | CAEC019.16 |
| 2 | List the classification of amplifiers based on frequency of operation | Remember | CAEC019.17 |
| 3 | State Miller's theorem. Specify its relevance in the analysis of a BJT amplifier. | Remember | CAEC019.16 |
| 4 | Discuss various possibilities of inter-stage coupling of amplifiers. | Understand | CAEC019.17 |
| 5 | List out the special features of Darlington pair and cascode amplifiers. State the areas where these amplifiers are used? | Remember | CAEC019.16 |
| 6 | Write the expression for lower 3 – dB frequency of an n – stage amplifier with non – interacting stages. | Remember | CAEC019.17 |
| 7 | Two stages of amplifier are connected in cascade. If the first stage has a decibel gain of 40 and second stage has an absolute gain of 20 then what is the overall gain in decibels. | Remember | CAEC019.16 |
| 8 | Why the overall gain of multistage amplifier is less than the product of gains of individual stages. | Understand | CAEC019.17 |
| 9 | List the main characteristics of a Darlington amplifier? | Understand | CAEC019.16 |
| 10 | Why direct coupling is not suitable for amplification of high frequency | Understand | CAEC019.17 |
| **PART-B(LONG ANSWER QUESTIONS)** | | | |
| 1 | Analyze general transistor amplifier circuit using h parameter model. Derive the expressions for AI, AV, Ri, R0, AIs, AVs. | Remember | CAEC019.16 |
| 2 | Draw the circuit of an emitter follower(simplified model), and derive the expressions for AI, Av, Ri, R0 in terms of CE parameters. | Remember | CAEC019.17 |
| 3 | Write the analysis of a CB amplifier circuit using h parameters. Derive the expressions for AI, AV, Ri, R0.(simplified model)? | Remember | CAEC019.16 |
| 4 | Write the analysis of a CE amplifier circuit using h parameters. Derive the expressions for AI, AV, Ri, R0. | Understand | CAEC019.17 |
| 5 | Compare the different types of coupling methods used in multistage amplifiers. | Remember | CAEC019.16 |
| 6 | Sketch two RC-coupled CE transistor stages. Show the middle and low frequency model for one stage. Write the expressions for current gains | Remember | CAEC019.17 |
| 7 | Draw the circuit diagram of cascode amplifier with and without biasing circuit. What is the advantages of this circuit | Remember | CAEC019.16 |
| 8 | Explain about different methods of Inter stage coupling in amplifiers. When 2- stages of identical amplifiers are cascaded, obtain the expressions for overall voltage gain, current gain and power gain | Understand | CAEC019.17 |
| 9 | Analysis for CE amplifier with emitter resistance? | Remember | CAEC019.16 |
| 10 | Draw the low frequency parameter equivalent circuit of a CE amplifier and explain the significance of each parameter. | Remember | CAEC019.17 |

| S. No | QUESTION | Blooms Taxonomy Level | Course Learning Outcome |
|---|---|---|---|
| **PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)** | | | |
| 1. | A CE amplifier is driven by voltage source with internal resistance Rs=800Ω.The load impedance RL=2k Ω. The h-parameters are hie=1.1K,hre=2.5*10-4,hfe=50,hoe=25μA/V. Compute AI,AV, AIs, Ri, Zo & Ap. | Remember | CAEC019.16 |
| 2 | A CB amplifier is driven by voltage source with internal resistance Rs=800Ω.The load impedance RL=2k Ω. The h-parameters are hib=22 Ω, hrb=3*10-4,hfb=-0.98,hoe=0.5μA/V. Compute AI,AV, AIs, Ri, Zo & Ap. | Remember | CAEC019.17 |
| 3 | A CC amplifier is driven by voltage source with internal resistance Rs=800Ω.The load impedance RL=2k Ω. The h-parameters are hic=1.1K Ω ,hrc=1,hfc=-51,hoc=25μA/V. Compute AI,AV, AIs, Ri, Zo & Ap. | Understand | CAEC019.16 |
| 4 | A CE amplifier is driven by voltage source with internal resistance Rs=500Ω.The load impedance RL=1k Ω. The h-parameters are hie=1.1K,hre=2.5*10-4,hfe=50,hoe=25μA/V. Compute AI,AV, Ri, Zo ? | Understand | CAEC019.17 |
| 5 | A CE-CC Amplifier uses RS=1KΩ, . RC1= RE2=4KΩ . The h-parameters hie=1.2K, hre=5*10-4,hfe=50,hoe=25μA/V, hic=1.2 Ω ,hrc=1,hfc=- 51,hoc=25μA/V. Compute individual & overall A I & AV, Ri, Ro & Rot . | Understand | CAEC019.16 |
| 6 | A CE-CB (cascode) Amplifier uses RS=1KΩ, . RC1=25KΩ, RE=100Ω ,R3=200KΩ R4=10KΩ The h-parameters hie=2K, hre=0,hfe=100,hoe=0. | Remember | CAEC019.17 |
| 7 | A CE amplifier is driven by voltage source with internal resistance Rs=600Ω,RL=1200Ω. The h-parameters are hie=1.1K,hre=2.5x10-4,hfe=50,hoe=25μA/V. Compute AI,AV, AIs, Ri, Zo & Rot? | Remember | CAEC019.16 |
| 8 | Draw the circuit of CE amplifier with emitter resistor RE. Draw it's equivalent circuit using Approximate model. Calculate AI,AV, Ri, Zo & Rot if Rs=600Ω, RL=1000Ω, RE=800Ω. The h-parameters are hie=1.2K,hre=3*10-4, hfe=50, hoe=25μA/V. | Remember | CAEC019.17 |
| 9 | Draw the circuit of CB amplifier. Draw it's equivalent circuit using Approximate model. Calculate AI,AV, Ri, Zo & Rot if Rs=900Ω, RL=2000Ω.The h-parameters are hie=1.1K,hre=2.5*10-4,hfe=50,hoe=24μA/V. | Understand | CAEC019.16 |
| 10 | Draw the circuit of CC amplifier. Draw it's equivalent circuit using Approximate model. Calculate AI,AV, Ri, Zo & Rot if Rs=500Ω, RL=2000Ω. The h-parameters are hie=1.1K,hre=2.6*10-4,hfe=54,hoe=26μA/V. | Understand | CAEC019.17 |

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