Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC017

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER-II

B.Tech VII Semester End Examinations, November - 2019

Regulations: R16

VLSI DESIGN

(ECE)

Time: 3 hours **Max. Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1.	a)	Define scaling factor? Explain different types of device parameters.	**[7M]**
	b)	An nMOS transistor is operating in saturation region with the following parameters. V_{GS} =5V, V_T=1.2V, W/L =10, $\mu_n C_{ox}$=110 μ A/V^2. Find transconductance of the device.	**[7M]**
2.	a)	Illustrate the relationship between *I*DS versus *V*DS of MOSFET	**[7M]**
	b)	Consider an nMOS transistor in a 65 nm process with a minimum drawn channel length of 50 nm (λ = 25 nm). Let W/L = 4/2 λ (i.e., 0.1/0.05 μm). In this process, the gate oxide thickness is 10.5 *A*. Estimate the high-field mobility of electrons to be 80 $cm^2/V\,s$ at 70°*C*. The threshold voltage is 0.3V. Plot I_{ds} vs. V_{DS} for V_{GS}= 0, 0.2, 0.4, 0.6, 0.8, and 1.0	**[7M]**

UNIT – II

3.	a)	Explain about NMOS fabrication Process with neat diagrams	**[7M]**
	b)	Interpret the Pull-up to pull-down ratio (*Z*pu/*Z*pd) for an nMOS inverter driven through one or more Pass Transistors.	**[7M]**
4.	a)	Explain the terms figure of merit of MOSFET and output conductance, using necessary equations.	**[7M]**
	b)	Explain different series and parallel combinations of pull-up and pull-down networks for NAND and NOR	**[7M]**

UNIT – III

5.	a)	Write a short notes on electron migration?	**[7M]**
	b)	Draw the nMOS diagram and stick diagram for **y=(AB + CD)^1**	**[7M]**
6.	a)	Explain the latch up in CMOS in detail with neat diagram	**[7M]**
	b)	Design a layout diagram for the pMOS logic Y= (AB+AC+BC)'.	**[7M]**

UNIT – IV

7.	a)	Draw and explain the functional block diagram of CPLD with it's applications.	**[7M]**
	b)	Design 4:1MUX using transmission gate.	**[7M]**
8.	a)	Explain briefly about FPGA interconnect routing procedures?	**[7M]**
	b)	Realize the function f =A+BC using pseudo –nMOS logic.	**[7M]**

UNIT – V

9.	a)	Discuss about dynamic transmission-gate edge-triggered registers.	**[7M]**
	b)	Explain about clocking strategies of VLSI design?	**[7M]**
10.	a)	Discuss about Zero/One detector.	**[7M]**
	b)	Draw the structure of a serial-parallel multiplier and explain it.	**[7M]**

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COURSE OBJECTIVES:

I	Have skills to use concepts of MOS devices for the fabrication of integrated chips (IC's).
II	Familiarize CMOS layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
III	Demonstrate the ability to design static CMOS combinational and sequential logic at the transistor level, including mask layout.
IV	Focus in selecting appropriate building blocks of data path for given system.

COURSE OUTCOMES (COs):

CO 1	Explore the basic operations of MOSFET, parameters to be considered which effects the operation of MOS, effect of scaling on MOS devices, how to overcome draw back.
CO 2	Understand various VLSI design styles, fabrication process of MOS, able to Analyze the inverter characteristics, understand the delay, noise margin and power dissipation of MOS transistor.
CO 3	Use Physical design rules to be followed for MOS designs, understand drawbacks of interconnects reliability issues and the effect of CMOS latch-up
CO 4	Understand various gate level designs, analyze various performance parameters like area, speed and capacitance and study the Fan-In and Fan-out.
CO 5	Understand design options for common datapath operators, various memories, low power memories. Analyze various timing issues, clocking strategies of VLSI designs and study various digital designs.

COURSE LEARNING OUTCOMES (CLOs):

AEC017.01	Understand fundamentals of MOS devices and its V-I characteristics.
AEC017.02	Analyze the effect of parasitic elements on MOS device, effect of threshold voltage MOSFET.
AEC017.03	Understand the importance and effect of scaling on MOS devices; analyze the latest trends in CMOS technology.
AEC017.04	Understand the basic CMOS nano technology and the importance of it.
AEC017.05	Understand the fabrications steps involved in the MOS transistor.
AEC017.06	Study various inverter characteristics of NMOS, CMOS.
AEC017.07	Understand the effect of delay, noise margin and power dissipation of MOS devices.
AEC017.08	Understand implementation of logic designs using MOS transistors series & parallel circuits.

AEC017.09	Study other logic families like pass transistor logic, Bi-CMOS logic, and various pull-up networks
AEC017.10	Understand to implement layers using stick diagram along with the color representation
AEC017.11	Study the design rules of transistors, wires , contacts and layouts with respect to width, length and spacing based on type of technology
AEC017.12	Understand effects on VLSI Interconnects and electron migration.
AEC017.13	Study the latch up problems and reliability issues of CMOS
AEC017.14	Understand various gate level designs for the logics and study about Fan-In and Fan-out.
AEC017.15	Analyze the effect of various capacitances of MOS devices on propagation delay and study about the reduction of RC values based on the choice of layers in the MOS devices.
AEC017.16	Understand the implementation strategies of VLSI design.
AEC017.17	Understand the design of programmable logic devices and analyze the speed and area tradeoffs.
AEC017.18	Understand data path subsystem designs, array subsystem designs
AEC017.19	Understand the operation of various static and dynamic latches and registers.
AEC017.20	Analyze the timing issues and the clock strategies of VLSI designs.
AEC017.21	Understand the purpose and operation of Low power memory Circuits
AEC017.22	Study various Synchronous and asynchronous circuit design; understand the operation of static and dynamic latches and registers.

MAPPING OF SEMESTER END EXAMINATION - COURSE OUTCOMES

SEE Question No.		Course Learning Outcomes		Course Outcomes	Blooms Taxonomy Level
1	a	AEC017.03	Understand the importance and effect of scaling on MOS devices; analyze the latest trends in CMOS technology.	CO 1	Understand
	b	AEC017.02	Analyze the effect of parasitic elements on MOS device, effect of threshold voltage MOSFET.	CO 1	Understand
2	a	AEC017.01	Understand fundamentals of MOS devices and its V-I characteristics.	CO 1	Understand
	b	AEC017.02	Analyze the effect of parasitic elements on MOS device, effect of threshold voltage MOSFET.	CO 1	Understand
3	a	AEC017.05	Understand the fabrications steps involved in the MOS transistor.	CO 2	Understand
	b	AEC017.06	Study various inverter characteristics of NMOS, CMOS.	CO 2	Remember
4	a	AEC017.07	Understand the effect of delay, noise margin and power dissipation of MOS devices.	CO 2	Understand
	b	AEC017.08	Understand implementation of logic designs using MOS Transistors series & parallel circuits.	CO 2	Understand
5	a	AEC017.12	Understand effects on VLSI Interconnects and electron migration.	CO 3	Understand
	b	AEC017.10	Understand to implement layers using stick diagram along with the color representation.	CO 3	Understand
6	a	AEC017.13	Study the latch up problems and reliability issues of CMOS.	CO 3	Understand
	b	AEC017.11	Study the design rules of transistors, wires , contacts and layouts with respect to width, length and spacing based on type of technology.	CO 3	Understand

7	a	AEC017.17	Understand the design of programmable logic devices and analyze the speed and area tradeoffs.	CO 4	Understand
	b	AEC017.14	Understand various gate level designs for the logics and Study about Fan-In and Fan-out.	CO 4	Understand
8	a	AEC017.17	Understand the design of programmable logic devices and analyze the speed and area tradeoffs.	CO 4	Understand
	b	AEC017.14	Understand various gate level designs for the logics and study about Fan-In and Fan-out.	CO 4	Understand
9	a	AEC017.19	Understand the operation of various static and dynamic latches and registers.	CO 5	Understand
	b	AEC017.20	Analyze the timing issues and the clock strategies of VLSI designs.	CO 5	Understand
10	a	AEC017.22	Study various Synchronous and asynchronous circuit design; static and dynamic latches and registers.	CO 5	Understand
	b	AEC017.22	Study various Synchronous and asynchronous circuit design; static and dynamic latches and registers.	CO 5	Understand

Signature of Course Coordinator **HOD, ECE**