INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Name	**:**	**VLSI Design**			
Course Code	**:**	**A60432**			
Regulation	**:**	**R15**			
Course Structure	**:**	**Lectures**	**Tutorials**	**Practicals**	**Credits**
		4	**1**	**-**	**4**
Class	**:**	**III B. Tech II Semester**			
Branch	**:**	**Electronics and Communication Engineering**			
Academic Year	**:**	**2017– 2018**			
Course Coordinator		**V. R. Seshagiri Rao, Professor, ECE.**			
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OBJECTIVES

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

S. No	Questions	Blooms Taxonomy Level	Course Outcome
	MID-I		
	UNIT-I **INTRODUCTION AND BASIC ELECTRICAL PROPPERTIES**		
	PART-A (SHORT ANSWER QUESTIONS)		
1	List the advantages of ICs.	Remember	1
2	Discuss the four generations of Integrated Circuits.	Understand	1
3	Describe BiCMOS Technology.	Understand	1
4	Illustrate the steps involved in twin-tub process.	Understand	1
5	State the different types of CMOS processes.	Remember	1
6	Explain the basic processing steps involved in BiCMOS process.	Remember	1
7	State Moore's law.	Remember	1
8	Describe enhancement mode and depletion mode of transistor.	Remember	1
9	List the advantages of CMOS process.	Remember	1

S. No	Questions	Blooms Taxonomy Level	Course Outcome
10	State why nMOS technology is preferred more than pMOS technology.	Remember	1
11	Describe Short Channel devices.	Remember	1
12	Explain about pull down device.	Understand	1
13	Explain about pull up device.	Understand	1
14	Describe the different operating regions for an MOS transistor.	Remember	2
15	Define threshold voltage of MOS transistor.	Remember	2
16	Demonstrate the transfer characteristics of CMOS inverter.	Remember	2
17	Describe channel length modulation.	Remember	1
18	Define latch up.	Remember	1
19	Demonstrate the CMOS inverter circuits.	Analyze	2
20	Demonstrate nMOS inverter circuit.	Understand	2
21	Explain pass transistor.	Understand	2
22	Demonstrate BiCMOS inverter circuit.	Analyze	2
23	Describe figure of merit.	Remember	2
PART-B (LONG ANSWER QUESTIONS)			
1	Explain the operation of NMOS enhancement transistor.	Understand	1
2	Explain about the body effect of MOS transistors.	Understand	1
3	Explain the silicon semiconductor fabrication process.	Understand	1
4	Explain the fabrication of PMOS transistor and its substrate fabrication Process.	Understand	1
5	Explain different fabrication process of CMOS transistor.	Understand	1
6	Explain the silicon semiconductor fabrication process.	Understand	1
7	Derive the threshold voltage for NMOS enhancement transistor.	Analyze	1
8	Derive the design equations for MOS devices.	Understand	1
9	Explain channel length modulation.	Understand	1
10	Explain BiCMOS fabrication in an n-well process.	Understand	1
11	Compare between CMOS and bipolar technologies.	Remember	1
12	Illustrate the relationship between I_{ds} versus V_{ds} of MOSFET.	Understand	1
13	Interpret the Pull-up to pull-down ratio (Z_{pu}/Z_{pd}) for an nMOS inverter driven by another nMOS inverter.	Analyze	1
14	Interpret the Pull-up to pull-down ratio (Z_{pu}/Z_{pd}) for an nMOS inverter driven through one or more Pass Transistors.	Analyze	1
15	Explain the various forms of pull-ups.	Understand	1
16	Explain what is latch up in CMOS and BiCMOS Susceptibility.	Understand	1
17	Differentiate the parameters of CMOS and Bipolar Technologies.	Remember	1
18	Explain BiCMOS inverter in all conditions.	Understand	2
19	Explain the latch up prevention techniques.	Remember	1
20	Illustrate the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics.	Analyze	2
21	Explain the terms figure of merit of MOSFET and output conductance, using necessary equations.	Remember	1
PART-C (ANALYTICAL QUESTIONS)			
1	Explain how a bipolar NPN transistor is included in n-well CMOS processing. Draw the cross section of BiCMOS.	Understand	1
2	Consider an nMOS transistor in a 65 nm process with a minimum drawn channel length of 50 nm (λ = 25 nm). Let W/L = 4/2 λ (i.e., 0.1/0.05 μm). In this process, the gate oxide thickness is 10.5 A. Estimate the high-field mobility of electrons to be 80cm^2/V s at 70°C. The threshold voltage is 0.3V. Plot I_{ds} vs. V_{ds} for V_{gs}= 0, 0.2, 0.4, 0.6, 0.8, and 1.0 V using the long-channel model.	Understand	1
3	Calculate the diffusion parasitic C_{db} of the drain of a unit-sized contacted	Understand	1

S. No	Questions	Blooms Taxonomy Level	Course Outcome
	nMOS transistor in a 65 nm process when the drain is at 0 V and again at V_{DD}=1.0 V. Assume the substrate is grounded. The diffusion region conforms to the design rules from Figure 2.8 with λ = 25 nm. The transistor characteristics are *CJ* = 1.2 fF/μm^2, *MJ* = 0.33, *CJSW* = 0.1 fF/μm, *CJSWG*=0.36 fF/μm, *MJSW* = *MJSWG* = 0.10, and 0 = 0.7 V at room temperature.		
4	Consider the nMOS transistor in a 65 nm process with a nominal threshold voltage of 0.3 V and a doping level of 8×10^{17} cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 0.6 V instead of 0?	Evaluate	1
5	What is the minimum threshold voltage for which the leakage current through an OFF transistor (V_{gs}=0) is 10^3 times less than that of a transistor that is barely ON (V_{gs}=V_t) at room temperature if n=1.5. One of the advantages of silicon-on insulator (SOI) processes is that they have smaller n. What threshold is required for SOI if n=1.3.	Remember	1
6	Consider an nMOS transistor in a 0.6 μm process with W/L = 4/2 λ (i.e., 1.2/0.6 μm). In this process, the gate oxide thickness is 100 A and the mobility of electrons is 350 cm2/V· s. The threshold voltage is 0.7 V. Plot I_{ds} vs. V_{ds} for V_{gs}=0, 1, 2, 3, 4, and 5 V.	Understand	1
7	Derive an equation for I_{dc} of an n channel process of twin well MOSFET operating in saturation region.	Understand	1
8	An nMOS transistor is operating in saturation region with the following parameters. V_{gs}=5V, V_{th}=1.2V, (W/L)=10, μC_{ox}=110μ A/V^2. Find transconductance of the device.	Remember	1
9	For a CMOS inverter, calculate the shift in the transfer characteristic curve when βn/ βp ratio is varied from 1/1 to 10/1.	Understand	1
10	Find gm and rds for an n-channel transistor with V_{gs}=1.2V, V_{th}=0.8V, (W/L)=10, μC_{ox}=92μ A/V^2 and V_{DS}=V_{eff} +0.5V. The output impedance constant=0.0953V^{-1}.	Understand	1
11	Draw the pass transistor arrangement for the logic X=ABC.	Remember	1
	UNIT-II **VLSI CIRCUIT DESIGN PROCESSES**		
PART-A (SHORT ANSWER QUESTIONS)			
1	Explain VLSI design flow.	Understand	3
2	Describe Stick Diagram.	Remember	3
3	List the uses of Stick diagram.	Remember	3
4	List the various types of color coding used in stick diagram.	Remember	3
5	Explain different MOS layers.	Understand	3
6	Sketch a stick diagram for 2 input nMOS NAND gate.	Remember	3
7	List the types of design rules.	Remember	3
8	Sketch a Transistor related design rules (Orbit 2 μm CMOS) minimum sizes and overlaps.	Remember	3
9	Sketch the aspects of λ-based design rules for contacts, including some factors contributing to higher yield/reliability.	Remember	3
10	Sketch the stick diagram for 2 input nMOS nor gate.	Remember	3
11	Describe Scaling.	Remember	3
12	Explain about transistor design rules for Nmos.	Understand	3
13	Describe layout diagram.	Remember	3
14	Sketch stick diagram for nMOS inverter.	Analyze	3
PART-B (LONG ANSWER QUESTIONS)			
1	Explain clearly the nMOS Design style with neat sketches.	Understand	3
2	Explain clearly the CMOS Design style with neat sketches.	Understand	3

S. No	Questions	Blooms Taxonomy Level	Course Outcome
3	(a) What is a stick diagram? Sketch the stick diagram and layout for a CMOS inverter. (b) What are design rules? Why is metal- metal spacing larger than poly–poly spacing.	Understand	3
4	Sketch the stick diagram for the NMOS implemented of the Boolean expression Y=AB+C.	Remember	3
5	Sketch a Schematic and Cell Layout with neat diagrams. Explain λ- based design rules for contact cuts and vias with neat diagram.	Remember	3
6	Draw the circuit schematic and stick diagram of CMOS 2-Input NAND Gate.	Remember	3
7	Sketch the transistor level diagram for the expression Y=AB+CD and also get the corresponding Stick diagram representation using CMOS logic.	Analyze	3
8	Define Scaling. What are the factors to be considered for transistor scaling?	Remember	3
9	Define constant voltage scaling and give necessary equations.	Remember	3
10	Explain with suitable examples how to design the layout of a gate to maximize performance and minimize area.	Remember	3
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)			
1	Sketch a stick diagram for a CMOS gate computing Y=A+B+C+D and estimate the cell width and height.	Understand	3
2	Design a layout diagram for the CMOS logic shown below Y□ □ □ A□ B·C□.	Analyze	3
3	Design a stick diagram for the CMOS logic shown below Y□ □ A□ B□ C.	Analyze	3
4	Design a stick diagram for two input pMOS NAND and NOR gates.	Analyze	3
5	Design a stick diagram for the CMOS logic for AB□ CD.	Analyze	3
6	Design a layout diagram for the pMOS logic Y□ A(B□ C.)	Analyze	3
7	Design a layout diagram for two input nMOS NAND gate.	Analyze	3
8	Design a stick diagram and layout for two input CMOS NAND gate indicating all the regions and layers.	Analyze	3
9	Draw the stick diagram and mask layout for a CMOS two input NOR gate.	Remember	3
UNIT-III GATE LEVEL DESIGN			
PART-A (SHORT ANSWER QUESTIONS)			
1	Give the different symbols for transmission gate representation.	Remember	4
2	What is pass transistor?	Understand	4
3	What is sheet resistance?	Remember	4
4	Define Rise time.	Understand	4
5	Define Fall time.	Remember	4
6	Define Delay time.	Remember	4
7	What are the other forms of CMOS logic?	Understand	4
8	Draw AND gate with pass transistors.	Remember	4
9	Explain why D latch is called level sensitive latch.	Understand	4
PART-B (LONG ANSWER QUESTIONS)			
1	Draw the CMOS implementation of 4-to-1 MUX using transmission gates.	Remember	4
2	Explain the VLSI design flow with a neat diagram.	Understand	4
3	Explain the Transmission gate and tri state inverter briefly.	Understand	4
4	Clearly explain the AOI implementation using CMOS design style with neat diagrams.	Understand	4
5	Design a 2-input multiplexer using CMOS transmission gates.	Analyze	4

S. No	Questions	Blooms Taxonomy Level	Course Outcome
6	Explain clocked CMOS logic and n-p CMOS logic. Mention their advantages and disadvantages.	Understand	4
7	Explain dynamic CMOS logic and give its advantages and disadvantages.	Understand	4
8	Explain CMOS domino logic and give its advantages and disadvantages.	Understand	4
9	Explain PSEUDO nMOS Logic give with advantages and disadvantages.	Understand	4
10	List the logical constraints of layers.	Remember	4
PART-C (ANALYTICAL QUESTIONS)			
1	Realize the function f=AB+CD using pseudo-nMOS logic.	Remember	4
2	Realize the function f =A+BC using pseudo –nMOS logic.	Remember	4
3	Derive the expression for rise and fall time of CMOS inverter. Comment on the expression derived.	Understand	4
4	Realize the function f=ABD+BCD using pseudo-nMOS logic.	Remember	4
5	Realize the function f =AB+CD using CMOS static logic.	Remember	4
6	Explain D latch using MUX and transmission gate.	Understand	4
7	Calculate ON resistance from VDD to GND for the given inverter, if n-channel sheet resistance is $2x10^4\Omega$/square.	Understand	4
8	Explain 4:1MUX using transmission gate.	Understand	4
MID -II			
UNIT-III GATE LEVEL DESIGN			
PART-A (SHORT ANSWER QUESTIONS)			
1	What is meant by wiring capacitance?	Remember	4
2	What is fan in?	Understand	4
3	What is fan out?	Understand	4
4	Draw OR gate with pass transistors.	Remember	4
5	Draw the circuit for inverter type super buffer.	Remember	4
6	Define BiCMOS drivers.	Remember	4
7	Define inter layer capacitance.	Remember	4
8	Define nMOS Super buffer?	Remember	4
PART-B (LONG ANSWER QUESTIONS)			
1	Derive the expression for time delay T_{sd} in case of MOSFET.	Analyze	4
2	Discuss the issues involved in driving large capacitive loads in VLSI circuit regions.	Understand	4
3	Describe three sources of wiring capacitances. Discuss the wiring Capacitance on the performance of a VLSI circuit.	Understand	4
4	Explain detail about choice of layers.	Understand	4
5	Discuss inverting and non-inverting Super Buffer.	Understand	4
6	Draw the CMOS implementation of 8-to-1 MUX using transmission gates.	Remember	4
7	Design a 4-input multiplexer using CMOS transmission gates.	Analyze	4
8	Explain the requirement and operation of pass transistors and transmission gates.	Understand	4
9	Describe three sources of wiring capacitances. Explain the effect of wiring capacitance of the performance of a VLSI circuit.	Understand	4
PART-C (ANALYTICAL QUESTIONS)			
1	Calculate the gate capacitance value of 5mm technology minimum size transistor with gate to channel capacitance value is 0.0004 pF/mm^2.	Understand	4
2	What is the problem of driving large capacitive loads? Explain a method to drive such load.	Understand	4
3	State the problem that arises when comparatively large capacitive loads are driven by inverters. Explain how super buffers can solve the problem.	Understand	4
4	Explain 2:1 multiplexer using transmission gate and tristate inverter.	Understand	4

S. No	Questions	Blooms Taxonomy Level	Course Outcome
5	Two NMOS inverters are cascaded to drive a capacitive load $C_L=14C_g$ as shown in figure. Calculate the pair delay V_{in} to V_{out} interms of Ƭ for the data given. Inverter A:$L_{p.u}=12\lambda$ $W_{p.u}=4\lambda$ $L_{p.d}=1\lambda$ $W_{p.d}=1\lambda$ Inverter B: $L_{p.u}=4\lambda$ $W_{p.u}=4\lambda$ $L_{p.d}=2\lambda$ $W_{p.d}=8\lambda$	Understand	4
6	Sketch a transistor level schematic for a CMOS 4- input NOR gate.	Understand	4
7	Two NMOS inverters are cascaded to drive a capacitive load $C_L=10C_g$ as shown in figure. Calculate the pair delay V_{in} to V_{out} interms of Ƭ for the data given. Inverter A:$L_{p.u}=10\lambda$ $W_{p.u}=4\lambda$ $L_{p.d}=1\lambda$ $W_{p.d}=1\lambda$ Inverter B: $L_{p.u}=4\lambda$ $W_{p.u}=4\lambda$ $L_{p.d}=2\lambda$ $W_{p.d}=4\lambda$	Understand	4
	UNIT-IV **DATA PAT SUB SYSTEMS**		
PART-A (SHORT ANSWER QUESTIONS)			
1	What is a data path subsystem?	Remember	5
2	What is a shifter?	Remember	5
3	What is the difference between shifter and barrel shifter?	Remember	5
4	Write the truth table for 1-bit full adder.	Remember	5
5	Draw the circuit of one detector with AND gates.	Remember	5
6	Draw the circuit of zero detector with AND gates.	Understand	5
7	What is comparator?	Remember	5
8	Draw the circuit of comparator.	Remember	5
9	What is parity generator?	Remember	5
10	What is the difference between synchronous and asynchronous counter.	Remember	5
11	Write categories of memory arrays.	Remember	5
12	What is RAM.	Understand	6
13	What is ROM.	Understand	6
14	What is Serial access memory.	Understand	6
15	What is Content Addressable Memory.	Understand	6
16	Draw the 6-Transistor SRAM cell.	Remember	6
17	Draw the 1-Transistor DRAM cell.	Remember	6
18	What are the different types of serial access memories.	Remember	6
19	What is flash memory?	Remember	6
20	What are the different types of ROMs?	Remember	6
21	Explain the principle of SRAM.	Understand	6
22	Discuss the advantages of SRAM.	Understand	6
23	Explain the principle of DRAM.	Understand	6
24	Discuss the advantages of Flash memory.	Understand	6

S. No	Questions	Blooms Taxonomy Level	Course Outcome
PART-B (LONG ANSWER QUESTIONS)			
1	Describe half adder and Full adder.	Understand	5
2	Draw the logic diagram of zero/one detector and explain its operation with the help of stick diagram.	Remember	5
3	Draw the schematic of Array Multiplier. Explain its principle and operation.	Remember	5
4	Explain the carry look ahead Adder.	Understand	5
5	Explain the design hierarchies and bring out which kind of approach is better to adopt for system design.	Remember	5
6	Describe briefly n-bit parallel adder.	Understand	5
7	Draw the structure of barrel shifter and explain its operation.	Remember	5
8	How Boolean functions are performed using MUX. Discuss 1-bit CMOS implementation of ALU.	Understand	5
9	Sketch the schematic of serial parallel multiplier and explain its operation.	Remember	5
10	Discuss synchronous and asynchronous counters.	Remember	5
11	Discuss in detail about classification of memory arrays.	Understand	6
12	Explain the memory cell read and write operation of 6T SRAM with neat sketches.	Understand	6
13	Explain the principles of SRAM and DRAM.	Understand	6
14	What are the advantages of SRAM and DRAM? Distinguish each property.	Remember	6
15	Explain the read and write operations of 1T DRAM memory cell.	Remember	6
16	Explain the read and write operations of 3T DRAM memory cell.	Remember	6
17	Explain about NAND based ROM design.	Remember	6
18	Explain about NOR based ROM design.	Remember	6
19	Discuss about different types of ROMs.	Remember	6
20	Explain various types of serial access memories with sketches.	Understand	6
21	What is content addressable memory and give any one application of it?	Understand	6
PART-C (ANALYTICAL QUESTIONS)			
1	Draw circuit diagram of one transistor with capacitor dynamic RAM and also draw its layout.	Remember	6
2	Draw the circuit diagram for 4X4 barrel sifter using complementary transmission gates and explain its shifting operation.	Remember	5
3	Design an Incrementer circuit using counter.	Analyze	5
4	Design ripple structure for one-zero detector circuit.	Analyze	5
5	Design a comparator using XNOR gates.	Analyze	5
6	Design sum and carry expressions of carry look ahead adder using nMOS Logic.	Analyze	5
7	Design a 4-bit array multiplier and implement using basic gates.	Analyze	5
8	Implement JK flip-flop using PROM.	Understand	6
9	Implement 2-bit comparator using PAL logic.	Understand	7
10	Draw and explain the antifuse structure for programming the PAL device.	Remember	7
11	Implement Y =A.C+AB +ACD using programmable logic array (PLA).	Understand	7
12	Implement Y =A.C+AB +ACD using programmable array logic (PAL).	Understand	7
13	Implement Y =A.C+AB +ACD using programmable logic read only memory (PROM).	Understand	6
14	Design a 1-bit full adder and implement the sum and carry expressions using PLA.	Analyze	7

S. No	Questions	Blooms Taxonomy Level	Course Outcome
UNIT-V SEMICONDUCTOR INTEGRATD CIRCUIT DESIGN AND CMOS TESTING			
PART-A (SHORT ANSWER QUESTIONS)			
1	Name the different types of ASICs.	Remember	7
2	Analyze full custom ASIC design.	Understand	7
3	Analyze the standard cell-based ASIC design.	Understand	7
4	Differentiate between channeled and channel less gate array.	Remember	7
5	Explain about FPGA.	Understand	8
6	Explain about Antifuse technology.	Understand	7
7	Explain about Programmable Interconnects.	Understand	7
8	List the steps in ASIC design flow.	Remember	7
9	Discuss the parameters influencing low power design.	Understand	7
10	Explain about CPLD.	Understand	7
11	State the levels at which testing of a chip can be done.	Remember	9
12	Discuss the categories of testing.	Understand	9
13	Explain functionality tests.	Understand	9
14	Explain manufacturing tests.	Understand	9
15	Discuss the defects that occur in a chip.	Understand	9
16	Explain about fault models.	Understand	9
17	Analyze Stuck–At fault.	Understand	9
18	Explain fault models with relevant examples.	Understand	9
19	Discuss about Observability.	Understand	9
20	Discuss about Controllability.	Understand	9
21	Explain various approaches in design for testability.	Understand	9
22	Mention the common techniques involved in ad hoc testing.	Remember	9
23	Analyze the scan-based test techniques.	Understand	9
24	Analyze the self-test techniques.	Understand	10
25	Discuss the applications of chip level test techniques.	Understand	10
26	Explain boundary scan.	Understand	10
27	Analyze Test access port.	Understand	10
28	Explain about Boundary scan register.	Understand	9
PART-B (LONG ANSWER QUESTIONS)			
1	Discuss the different methods of programming of PALs.	Understand	7
2	Distinguish PLAs, PALs, CPLDs, FPGAs, and standard cells in all respects.	Remember	8
3	Explain about the principle and operation of FPGAs. What are its applications?	Understand	8
4	Draw the schematic of PLA and explain its principle of operation.	Remember	7
5	What are the advantages of PLAs?	Understand	7
6	Draw the schematic and examine how Full Adder can be implemented using PLAs.	Remember	7
7	Explain about configurable FPGA based I/O blocks.	Understand	8
8	Design JK Flip flop circuit using PLA.	Analyze	7
9	Explain semicustom design approach of an IC.	Understand	7
10	Compare semicustom and full custom designs of an IC.	Remember	7
11	Explain the various DFT techniques.	Understand	9
12	Explain system-level test techniques.	Remember	9
13	Explain about memory-self test with the help of a schematic.	Understand	9
14	Analyze the issues to be considered while implementing BIST and explain each.	Remember	9
15	Explain how layout design can be done for improving testability.	Remember	9
16	Explain about different fault models in VLSI testing with examples.	Remember	9

S. No	Questions	Blooms Taxonomy Level	Course Outcome
17	Analyze any TWO a) DFT b) BIST c) Boundary scan Testing.	Remember	9
18	Explain fault models.	Understand	9
19	Explain ATPG.	Understand	9
20	Briefly explain a) Fault grading & fault b) simulation delay fault testing c) Statistical fault analysis.	Understand	9
21	Discuss scan-based test techniques.	Understand	10
22	Explain Ad-Hoc testing and chip level test techniques.	Remember	10
23	Explain self-test techniques.	Remember	10
24	Explain a) BILBO b) TAP controller c) Observability d) Controllability.	Understand	10
PART-C (ANALYTICAL QUESTIONS)			
1	Draw the basic structure of parallel scan and explain how it reduces the long scan chains.	Understand	9
2	Explain how an improved layout can reduces faults in CMOS circuits.	Understand	10
3	Draw the state diagram of TAP controller and explain how it provides the control signals for test data and instruction register.	Understand	10
4	A sequential circuit has ‘n’ inputs and ‘m’ storage devices. To test this circuit how many test vectors are required?	Understand	10
5	How IDDQ testing is used to test the bridge faults?	Understand	10
6	What is ATPG? Explain a method of generation of test vector.	Understand	10

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HEAD OF THE DEPARTMENT,

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