INSTITUTE OF AERONAUTICAL ENGINEERING

(**Autonomous**)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Name	:	**VLSI TESTING**
Course Code	:	**AEC804**
Class	:	**B. Tech VI Semester**
Branch	:	**ECE**
Year	:	**2018 – 2019**
Course Coordinator	:	**Mr. D Khalandar Basha, Assistant Professor, ECE Department**
Course Faculty	:	**Mr. D Khalandar Basha, Assistant Professor, ECE Department**

I. COURSE OBJECTIVES:

The course should enable the students to:

S. No	Description
I	Understand the design methods for digital systems.
II	Understand the design of sequential circuits.
III	Illustrate the fault classes and models.
IV	Learn to generate the test cases using conventional methods.
V	Study designing of PLAs and its minimization.

II. COURSE LEARNING OUTCOMES

Students, who complete the course, will have demonstrated the ability to do the following

AEC001.01	Apply knowledge of digital systems, Sequential Circuit Design and design of digital logic circuits
AEC001.02	Explain fault modeling and classes.
AEC001.03	Apply knowledge of different algorithms for generating test patterns.
AEC001.04	Detect states and faults in sequential circuits.
AEC001.05	Explain PLA minimization and testing.
AEC001.06	Analyze an asynchronous sequential machines
AEC001.07	Explain the designing principles of various digital systems
AEC001.08	Analyze a given digital system and decompose it into logical blocks involving both combinational and sequential circuit elements.
AEC001.09	Explain Reduction of state tables and state assignments.
AEC001.10	Describe the Fault Modeling and Test pattern Generation methods.
AEC001.11	Describe PLA minimization and testing

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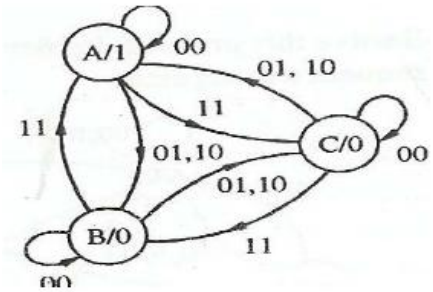
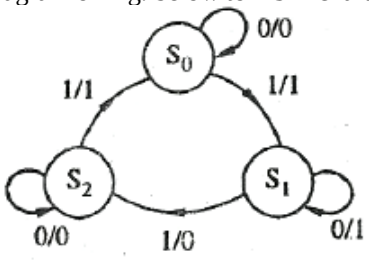
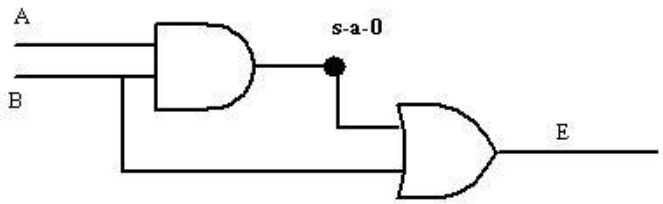
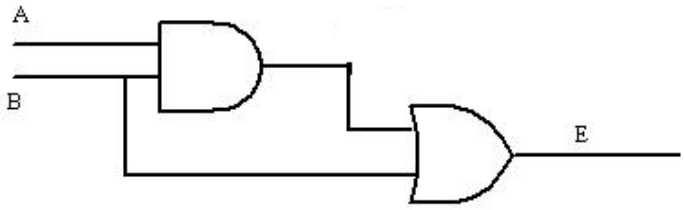
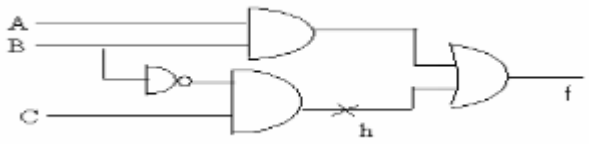
UNIT-I DESIGN OF DIGITAL SYSTEMS			
PART – A (SHORT ANSWER QUESTIONS)			
S. No	**Question**	**Blooms Taxonomy level**	**CLOs**
1	Define Melay machine.	Remember	AEC804.01
2	Define Moore machine.	Understand	AEC804.01
3	Differentiate Melay machine and Moore machine.	Understand	AEC804.01
4	Write about equivalent ASM charts with an example?	Understand	AEC804.02
5	What is VHDL stands for?	Understand	AEC804.03
6	List principal component of an ASM chart?	Remember	AEC804.02
7	Differentiate Concurrent statements and sequential statements?	Remember	AEC804.03
8	What is state diagram?	Remember	AEC804.04
9	How can states can be reduced in a state diagram?	Remember	AEC804.04
10	What are the advantages of one hot assignment?	Understand	AEC804.04
11	Which code is followed for one hot assignment?	Remember	AEC804.04
PART – B (LONG ANSWER QUESTIONS)			
1	Draw a Moore state machine that detects a sequence of 1010 and that asserts a logical 1 at the output during the last state of the sequence.	Remember	AEC804.01
2	Define simulation and synthesis.	Understand	AEC804.03
3	Draw the state diagram for and gate	Remember	AEC804.04
4	Draw the state diagram for a JK flip flop. The inputs for the JK flip flop are J, K, Q_n.	Understand	AEC804.04
5	Draw the state diagram for full adder.	Remember	AEC804.04
6	Write state table for 3-bit counter.	Understand	AEC804.04
7	Write the state table for 3bit binary to gray code converter.	Understand	AEC804.04
8	Convert the state diagram of Fig. below to ASM chart. 	Understand	AEC804.02
9	Draw an ASM chart to describe a mealy state machine that detects a sequence of 101 and that asserts a logical 1 at the output during the last state of the sequence.	Understand	AEC804.02
10	Convert the state diagram of Fig. below to ASM chart 	Understand	AEC804.02
UNIT-II SEQUENTIAL CIRCUIT DESIGN			
PART - A (SHORT ANSWER QUESTIONS)			
1	What is FPGA stands for?	Remember	AEC804.07
2	Define reconfiguration.	Remember	AEC804.07

3	How many address lines are required for accessing any memory location of 256x8 ROM?	Understand	AEC804.05
4	Differentiate combinational circuits and sequential circuits?	Remember	AEC804.05
5	What is an iterative circuit?	Understand	AEC804.05
6	What is CPLD stands for?	Understand	AEC804.06
7	How much can be interfaced for a processor with 15 address lines?	Understand	AEC804.05
8	What is EEPROM?	Understand	AEC804.05
9	What is a LUT in FPGA?	Remember	AEC804.07
10	What is PLA stands for?	Remember	AEC804.05
11	Illustrate internal circuit of PLA?	Remember	AEC804.05
	PART– B (LONG ANSWER QUESTIONS)		
1	Differentiate PLA and PAL.	Understand	AEC804.05
2	What are the advantages of Gate arrays and give any two examples for gate arrays?	Remember	AEC804.06
3	Explain the functionality of a 3 bit LUT with an example?	Remember	AEC804.07
4	Design a ROM to function as full adder?	Understand	AEC804.05
5	Design a ROM to function as JK flip flop?	Understand	AEC804.05
6	Design a ROM to function as 2 to 4 decoder?	Understand	AEC804.05
7	Differentiate CPLDs and FPGAs?	Remember	AEC804.06
8	Explain the functionality of IO block of FPGA?	Understand	AEC804.07
9	Explain about the macro cell in a CPLD?	Remember	AEC804.06
10	Explain ROM internal structure with a neat sketch?	Understand	AEC804.05
	UNIT-III **FAULT MODELING**		
	PART –A (SHORT ANSWER QUESTIONS)		
1	What is meant by transition faults?	Remember	AEC804.08
2	Define bridging faults.	Understand	AEC804.09
3	Illustrate stuck at faults	Understand	AEC804.08
4	What is meant by intermittent faults?	Understand	AEC804.08
5	How many stuck faults can occur for a 2 input AND gate?	Understand	AEC804.09
6	What is meant by fault equivalence?	Understand	AEC804.08
	CIE II		
1	What is fault sensitization?	Understand	AEC804.10
2	What is fault propagation?	Understand	AEC804.10
3	What is the significance of Kohavi algorithm?	Understand	AEC804.11
4	Define a diagnosable sequential machine	Remember	AEC804.10
5	List the different types of faults in a digital circuits	Understand	AEC804.10
	PART – B (LONG ANSWER QUESTIONS)		
1	Find the test vector(s) to detect SA0 fault at the output of a two input AND gate?	Understand	AEC804.08
2	Find the test vector(s) to detect SA1 fault at the output of a two input OR gate?	Remember	AEC804.08
3	Find the test vector(s) to detect SA1 fault at the output of a two input NAND gate?	Remember	AEC804.08
4	Find the test vector(s) to detect SA0 fault at the output of a two input NOR gate?	Understand	AEC804.08
5	Explain the terms observability and controllability?	Remember	AEC804.09
	CIE II		
1	Using path sensitization generate test pattern for the s-a-0 fault in the circuit given below? 	Understand	AEC804.10
2	How to detect the fault at input B using Boolean difference method?	Remember	AEC804.10

			
3	Find the test vectors of all SA0 and SA1 faults of the circuit function. F=x1x2+x1x3'x4'+x2x4 using Kohavi algorithm.	Understand	AEC804.11
4	Draw the circuit which realizes the logic function z= x1 x2 +x3 x4 using AND and OR gates. For the circuits realized above, determine a test vector which denotes SA0 fault on the line 'x2'.	Understand	AEC804.10
5	With an example, Explain the procedure involved in the path sensitization technique.	Understand	AEC804.10
UNIT-IV TEST PATTERN GENERATION			
PART – A (SHORT ANSWER QUESTIONS)			
1	What is fault coverage?	Remember	AEC804.12
2	Define Exhaustive testing	Remember	AEC804.12
3	Differentiate Ones count compression and transition count compression	Remember	AEC804.12
4	Relate fault coverage and no. of faults.	Understand	AEC804.12
5	How a transition count is used to test faults.	Remember	AEC804.12
6	Give the classification of faults that may occur in digital circuits with examples	Understand	AEC804.13
7	Construct a truth table for an XOR function of two input using the five logic values 0, 1, x, D, and D'.	Understand	AEC804.13
8	Brief about Ones count compression	Remember	AEC804.12
9	What is transition count compression	Remember	AEC804.12
10	Define the term 'failure'?	Understand	AEC804.12
11	Define the term 'fault'?	Remember	AEC804.12
PART – B (LONG ANSWER QUESTIONS)			
1	Discuss in brief about D-algorithm.	Remember	AEC804.13
2	Apply D-algorithm to detect the SA0 fault in the given circuit and derive the test vectors. 	Understand	AEC804.13
3	Describe the algorithmic steps involved in PODEM	Remember	AEC804.13
4	Explain the transition count testing method with an example.	Understand	AEC804.12
5	Explain signature analysis with an example.	Understand	AEC804.13
6	Explain in detail different test pattern generation method.	Understand	AEC804.12
7	Explain the test vector for bridging faults with an example.	Remember	AEC804.12
8	Explain how LFSR is used in signature analysis compression technique.	Remember	AEC804.13
9	For an autonomous LFSR show that if it's initial state is not all 0 state then it will never enter the all 0 state.	Remember	AEC804.13
UNIT-V PROGRAMMING LOGIC ARRAYS			
PART – A (SHORT ANSWER QUESTIONS)			
1	List out and explain briefly about the faults that may occur in PLAs.	Remember	AEC804.14
2	Draw the block diagram of PLA.	Remember	AEC804.14
3	Give the diagram of three inputs, five product terms and four outputs of PLA structure	Remember	AEC804.14
4	Explain how to test a PLA circuits?	Remember	AEC804.14
5	List out the different types of fault models and fault types in a PLA.	Remember	AEC804.14
6	Realize F1 using PLA. Give the PLA table and interconnection diagram for the PLA. F1(a, b, c) = $\sum$m(1,2,4,5,6).	Remember	AEC804.14

7	List the advantages of PLA.	Remember	AEC804.14
8	What is PLA stands for?	Remember	AEC804.14
9	Illustrate internal circuit of PLA?	Remember	AEC804.14
10	Realize F1 using PLA. Give the PLA table and interconnection diagram for the PLA. F1(a, b, c) = ∑ m(1,3,5,7)	Remember	AEC804.14
	PART – B (LONG ANSWER QUESTIONS)		
1	Draw the schematic for PLA and explain the principle. What are the advantages of PLD's	Remember	AEC804.14
2	Give the PLA realization of the following functions using a PLA with 5 inputs, 4 outputs and 8 AND gates. $f_1(A,B,C,D,E) = \sum m(0,1,2,3,11,12,13,14,15,16,17,18,19,27,28,29,30,31)$	Remember	AEC804.14
3	Design a 3 bit BCD to grey code converter and realize the circuit using PLA.	Understand	AEC804.14
4	Design a 3 bit grey code to BCD converter and realize the circuit using PLA.	Understand	AEC804.14
5	Explain the procedure steps of PLA folding algorithm and illustration of algorithm with suitable example.	Remember	AEC804.15
6	Find the minimized PLA of the following output Boolean function by a PLA minimizer. f1 = (2,4,5,6,7,10,14,15): f2 = (4,5,7,11,15)	Understand	AEC804.15
7	Give the PLA realization of the following functions using a PLA with 5 inputs, 4 outputs and 8 AND gates $f_2(A,B,C,D,E) = \sum m(4,5,6,7,8,9,10,11,20,21,22,23,30)$	Understand	AEC804.14
8	Design a PLA to function as full adder?	Remember	AEC804.14
9	Design a PLA to function as JK flip flop?	Remember	AEC804.14
10	Design a PLA to function as 2 to 4 decoder?	Remember	AEC804.14

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