INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Name	:	VLSI TESTING
Course Code	:	AEC804
Class	:	B. Tech VI Semester
Branch	:	ECE
Year	:	2018 – 2019
Course Coordinator	:	Mr. D Khalandar Basha, Assistant Professor, ECE Department
Course Faculty	:	Mr. D Khalandar Basha, Assistant Professor, ECE Department

I. COURSE OBJECTIVES:

The course should enable the students to:

S. No	Description
Ι	Understand the design methods for digital systems.
II	Understand the design of sequential circuits.
III	Illustrate the fault classes and models.
IV	Learn to generate the test cases using conventional methods.
V	Study designing of PLAs and its minimization.

II. COURSE LEARNING OUTCOMES

Students, who complete the course, will have demonstrated the ability to do the following

AEC001.01	Apply knowledge of digital systems, Sequential Circuit Design and design of digital logic circuits
AEC001.02	Explain fault modeling and classes.
AEC001.03	Apply knowledge of different algorithms for generating test patterns.
AEC001.04	Detect states and faults in sequential circuits.
AEC001.05	Explain PLA minimization and testing.
AEC001.06	Analyze an asynchronous sequential machines
AEC001.07	Explain the designing principles of various digital systems
AEC001.08	Analyze a given digital system and decompose it into logical blocks involving both combinational and sequential circuit elements.
AEC001.09	Explain Reduction of state tables and state assignments.
AEC001.10	Describe the Fault Modeling and Test pattern Generation methods.
AEC001.11	Describe PLA minimization and testing



TUTORIAL QUESTION BANK

	UNIT-I DESIGN OF DIGITAL SYSTEMS		
ART	- A (SHORT ANSWER QUESTIONS)		
S. No	Question	Blooms Taxonomy level	CLOs
1	Define Melay machine.	Remember	AEC804.01
2	Define Moore machine.	Understand	AEC804.01
3	Differentiate Melay machine and Moore machine.	Understand	AEC804.01
4	Write about equivalent ASM charts with an example?	Understand	AEC804.02
5	What is VHDL stands for?	Understand	AEC804.03
6	List principal component of an ASM chart?	Remember	AEC804.02
7	Differentiate Concurrent statements and sequential statements?	Remember	AEC804.03
8	What is state diagram?	Remember	AEC804.04
9	How can states can be reduced in a state diagram?	Remember	AEC804.04
10	What are the advantages of one hot assignment?	Understand	AEC804.04
11	Which code is followed for one hot assignment?	Remember	AEC804.04
	PART – B (LONG ANSWER QUESTIONS)		
1	Draw a Moore state machine that detects a sequence of 1010 and that asserts a logical 1 at the output during the last state of the sequence.	Remember	AEC804.01
2	Define simulation and synthesis.	Understand	AEC804.03
3	Draw the state diagram for and gate	Remember	AEC804.04
4	Draw the state diagram for a JK flip flop. The inputs for the JK flip flop are J, K, Q_n .	Understand	AEC804.04
5	Draw the state diagram for full adder.	Remember	AEC804.04
6	Write state table for 3-bit counter.	Understand	AEC804.04
7	Write the state table for 3bit binary to gray code converter.	Understand	AEC804.04
	A/1 00 01, 10 11 01,10 C/0 00 B/0 11 60		
9	Draw an ASM chart to describe a mealy state machine that detects a sequence of 101 and that asserts a logical 1 at the output during the last state of the sequence.	Understand	AEC804.02
10	Convert the state diagram of Fig. below to ASM chart $1/1$ S_0 $1/1$ $1/1$ S_2 S_1	Understand	AEC804.02
	0/0 1/0 0/1 UNIT-II SEQUENTIAL CIRCUIT DESIGN PART - A (SHORT ANSWER QUESTIONS)		
1	What is FPGA stands for?	Remember	AEC804.07
	Define reconfiguration.	Remember	AEC804.07

3	How many address lines are required for accessing any memory location	Understand	AEC804.05
4	of 256x8 ROM?	Demessiehen	AEC904.05
4	Differentiate combinational circuits and sequential circuits?	Remember	AEC804.05
5	What is an iterative circuit?	Understand	AEC804.05
6	What is CPLD stands for?	Understand	AEC804.06 AEC804.05
7	How much can be interfaced for a processor with 15 address lines?	Understand	
<u>8</u> 9	What is EEPROM?	Understand	AEC804.05
10	What is a LUT in FPGA? What is PLA stands for?	Remember Remember	AEC804.07 AEC804.05
10	Illustrate internal circuit of PLA?	Remember	AEC804.05 AEC804.05
11	PART- B (LONG ANSWER QUESTIONS)	Kellieliidei	AEC 004.03
- 1	× × ×	XX 1 . 1	150004.05
1	Differentiate PLA and PAL.	Understand	AEC804.05
2	What are the advantages of Gate arrays and give any two examples for gate arrays?	Remember	AEC804.06
3	Explain the functionality of a 3 bit LUT with an example?	Remember	AEC804.07
4	Design a ROM to function as full adder?	Understand	AEC804.05
5	Design a ROM to function as JK flip flop?	Understand	AEC804.05
6	Design a ROM to function as 2 to 4 decoder?	Understand	AEC804.05
7	Differentiate CPLDs and FPGAs?	Remember	AEC804.06
8	Explain the functionality of IO block of FPGA?	Understand	AEC804.07
9	Explain about the macro cell in a CPLD?	Remember	AEC804.06
10	Explain ROM internal structure with a neat sketch?	Understand	AEC804.05
	UNIT-III FAULT MODELING		
	PART -A (SHORT ANSWER QUESTIONS)		
1	What is meant by transition faults?	Remember	AEC804.08
2	Define bridging faults.	Understand	AEC804.09
3	Illustrate stuck at faults	Understand	AEC804.08
4	What is meant by intermittent faults?	Understand	AEC804.08
5	How many stuck faults can occur for a 2 input AND gate?	Understand	AEC804.09
6	What is meant by fault equivalence?	Understand	AEC804.08
1		XX 1 4 1	AEC004.10
1	What is fault sensitization?	Understand	AEC804.10
2	What is fault propagation?	Understand	AEC804.10
3	What is the significance of Kohavi algorithm?	Understand	AEC804.11
4	Define a diagnosable sequential machine	Remember	AEC804.10
5	List the different types of faults in a digital circuits	Understand	AEC804.10
	PART – B (LONG ANSWER QUESTIONS)	I I.a. da nata a d	AEC904.09
1	Find the test vector(s) to detect SA0 fault at the output of a two input AND gate?	Understand	AEC804.08
2	Find the test vector(s) to detect SA1 fault at the output of a two input OR gate?	Remember	AEC804.08
3	Find the test vector(s) to detect SA1 fault at the output of a two input NAND gate?	Remember	AEC804.08
4	Find the test vector(s) to detect SA0 fault at the output of a two input NOR gate?	Understand	AEC804.08
5		D 1	AEC804.09
5	Explain the terms observability and controllability?	Remember	AEC 804.09
	CIE II		
1		Understand	AEC804.09 AEC804.10
	CIE II Using path sensitization generate test pattern for the s-a-0 fault in the		
	CIE II Using path sensitization generate test pattern for the s-a-0 fault in the circuit given below?		
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	CIE II Using path sensitization generate test pattern for the s-a-0 fault in the circuit given below? A B B B B B B B B B B		

3 Find the test vectors of all SA0 and SA1 faults of the circuit function. Understand AEC804.11 4 Draw the circuit which realizes the logic function z x I x 2 +x3 x4 using AND and OR gates. For the circuit stellize dabove, determine a test vector which denotes SA0 fault on the line 'x2'. Understand AEC804.10 5 With an example. Explain the procedure involved in the path sensitization technique. UNIT-IV Network of the circuit which ends the path sensitization technique. AEC804.10 1 What is fault coverage? Remember AEC804.12 AEC804.12 3 Differentiate Ones count compression and transition count compression Remember AEC804.12 4 Relate full coverage and no. of faults that may occur in digital circuits with cartand AEC804.13 Ce804.12 5 How a transition count is used to test faults. Remember AEC804.13 6 Give the classification of faults that may occur in digital circuits with cartand AEC804.13 10 Define the term 'failure'? Understand AEC804.13 11 Define the term 'failure'? Understand AEC804.12 12 Optime the term 'failure'? Understand AEC804.13 13 Discuss in brief about D-algorithm. Receed4.12 14 Define the term 'failure'? Understand AEC804.13		A		
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	5	List out the different types of fault models and fault types in a PLA.		AEC804.14
for the PLA. $F1(a, b, c) = \sum m(1, 2, 4, 5, 6)$.	6		Remember	AEC804.14
		for the PLA. $F1(a, b, c) = \sum m(1, 2, 4, 5, 6)$.		

7	List the advantages of PLA.	Remember	AEC804.14
8	What is PLA stands for?	Remember	AEC804.14
9	Illustrate internal circuit of PLA?	Remember	AEC804.14
10	Realize F1 using PLA. Give the PLA table and interconnection diagram	Remember	AEC804.14
	for the PLA. $F1(a, b, c) = \sum m(1,3,5,7)$		
	PART – B (LONG ANSWER QUESTIONS)		
1	Draw the schematic for PLA and explain the principle. What are the	Remember	AEC804.14
	advantages of PLD's		
	Give the PLA realization of the following functions using a PLA with 5	Remember	AEC804.14
2	inputs, 4 outputs and 8 AND gates.		
	$f_1(A, B, C, D, E) = \sum m(0, 1, 2, 3, 11, 12, 13, 14, 15, 16, 17, 18, 19, 27, 28, 29, 30, 31)$		
3	Design a 3 bit BCD to grey code converter and realize the circuit using	Understand	AEC804.14
	PLA.		
4	Design a 3 bit grey code to BCD converter and realize the circuit using	Understand	AEC804.14
	PLA.		
5	Explain the procedure steps of PLA folding algorithm and illustration of	Remember	AEC804.15
	algorithm with suitable example.		
	Find the minimized PLA of the following output Boolean function by a	Understand	AEC804.15
6	PLA minimizer. $f1 = (2,4,5,6,7,10,14,15)$: $f2 = (4,5,7,11,15)$		
7	Give the PLA realization of the following functions using a PLA with 5	Understand	AEC804.14
	inputs, 4 outputs and 8 AND gates		
	$\hat{f}_2(A, B, C, D, E) = \sum m(4, 5, 6, 7, 8, 9, 10, 11, 20, 21, 22, 23, 30)$		
8	Design a PLA to function as full adder?	Remember	AEC804.14
9	Design a PLA to function as JK flip flop?	Remember	AEC804.14
10	Design a PLA to function as 2 to 4 decoder?	Remember	AEC804.14

HOD, ECE