INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNIACTION ENGINEERING

QUESTION BANK

Course Name	:	**LINEAR AND DIGITAL INTEGRATED CIRCUITS APPLICATIONS**
Course Code	:	**A50425**
Class	:	III - B. Tech
Branch	:	ECE
Year	:	2017-18
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OBJECTIVES

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

S.No	QUESTION	Blooms taxonomy level	Course Outcome
	UNIT-I **OPERATIONAL AMPLIFIER** **SHORT ANSWER QUESTIONS**		
1	Mention the advantages of integrated circuits.	Remember	1
2	List the applications of IC 741.	Understand	1
3	What is the purpose of IC 741	Understand	1
4	Define an operational amplifier.	Remember	1
5	Mention the characteristics of an ideal op-amp.	Analyze	1
6	Define input offset voltage	Remember	1
7	What are the applications of current sources?	Analyze	1
8	Define sensitivity of an op-amp.	Remember	1
9	What is slew rate? Discuss the methods of improving slew rate.	Understand	1,2
10	Explain pole zero compensation and frequency compensation in op-amp.	Remember	1
11	Define band gap reference? Explain in detail about the reference circuit	Remember	1
12	Briefly explain the method of using constant current bias for increasing CMRR in differential?	Remember	1
13	Explain the operation of a Schmitt trigger circuit.	Analyze	1,2
14	Why do we use R_{comp} resistor?	Understand	1
15	Define thermal drift?	Understand	1
16	Draw the circuit of lossy integrator showing initial conditions?	Analyze	1,2
17	Explain why integrators are preferred over differentiators in analog	Analyze	2

	computers.		
18	What is the function of voltage regulator?	Analyze	2
19	What voltage options are available in 78xx and 79xx voltage regulators?	Understand	2
20	Sketch the inverting and non inverting comparators using op-amp.	Understand	2
	LONG ANSWER QUESTIONS		
1	Explain the operation of a Schmitt trigger circuit using IC 741.	Understand	1
2	Explain practical integrator circuit using IC 741.	Analyze	1
3	Explain the internal structure of voltage regulator IC 723. Also draw a low voltage Regulator circuit using IC 723andexplain its operation.	Analyze	2
4	Explain the following terms in an OP-AMP. 1. Input Bias current 2. Input offset voltage 3. Input offset current	Remember	2
5	Explain non inverting comparator using op-amp.	Understand	3
6	Derive the gain for non inverting op-amp.	Remember	2
7	Write a technical note on frequency response characteristics of differential amplifier. State the importance of frequency compensation.	Understand	2
8	What is t instrumentation amplifier? What are the required parameters of an instrumentation amplifier? Explain the working of instrumentation amplifier with neat circuit diagram.	Understand	1
9	Explain various DC and AC characteristics of an op.amp. Distinguish between ideal and practical characteristics.	Understand	1
10	With circuit and waveforms explain the application of OPAMP as differentiator and write the advantages of practical differentiator.	Remember	1
	ANALYTICAL QUESTIONS		
1	An op-amp with a slew rate = 0.5V/μS is used as an inverting amplifier to obtain a gain of 100. The voltage gain Vs frequency characteristic of the amplifier is flat up to 10 KHz. Determine i. The maximum peak-to-peak input signal that can be applied without any distortion to the output ii. The maximum frequency of the input signal to obtain a sine wave output of 2V peak.	Analyze	2
2	Design a Schmitt trigger for UTP =0.5v and LTP = -0.5V.assume necessary data.	Evaluate	3
3	Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1 KHz. If a sine wave of 1V peak at 1000 Hz is applied to this differentiator draw the output waveforms.	Evaluate	2
4	Determine the output voltage of the differential amplifier having input voltages V1=1mV and V2=2 mV. The amplifier has a differential gain of 5000 and CMRR 1000.	Remember	2
5	Draw the output waveform for a sine wave of 1vpeak at 100Hzapplied to the differentiator.	Evaluate	2
6	Design an op-amp differentiator that will differentiate an Input signal with fmax = 100Hz	Remember	2
7	Find R1 and R_f in the lossy integrator so that the peak gain is 20dB and the gain is 3db down from its peak when ω = 10,000 rad/sec. use a capacitance of 0.01micro farads.	Evaluate	2
8	Design a Schmitt trigger for UTP =2V and LTP = -2V.assume necessary data.	Evaluate	3
9	Design an op-amp differentiator that will differentiate an Input signal with fmax = 1000Hz	Analyze	2
10	Find R1 and R_f in the lossy integrator so that the peak gain is 20dB and the gain is 3db down from its peak when ω = 1,000 rad/sec. use a capacitance of 0.1micro farads.	Evaluate	2
	UNIT -2 **OP-AMP, IC -555 & IC 565 APPLICATIONS** **SHORT ANSWER QUESTIONS**		

1	Why active filters are preferred?	Remember	4
2	What is meant by cut off frequency of a high pass filter and how it is found out in a first order high pass filter	Understand	4
3	List the applications of 555 timer in monostable mode of operation	Remember	5
4	Define 555 IC?	Remember	5
5	List the basic blocks of IC 555 timer?	Remember	5
6	Define VCO.	Remember	6
7	What does u mean by PLL?	Understand	6
8	List the applications of 565 PLL	Apply	6
9	Define lock range in PLL.	Understand	6
10	Define capture range in PLL.	Apply	6
11	Define pull-in time in PLL.	Understand	6
12	Draw a circuit to for converting a square wave into a series of positive pulses.	Understand	5
13	What is the difference between triangular and sawtooth wave.	Understand	5
14	Define an electronic filter.	Remember	4
15	Define pass band and stop band of a filter.	Remember	4
LONG ANSWER QUESTIONS			
1	Design a second order low pass filter.	Evaluate	4
2	Draw the circuit of a 1st order low pass filter and derive its transfer function.	Analyze	4
3	Explain the functional block diagram of 555timer.	Evaluate	5
4	Explain working of PLL using appropriate block diagram.	Evaluate	6
5	Draw the block diagram of an Astable multivibrator using 555timer and derive an expression for its frequency of oscillation.	Evaluate	5
6	Draw the block diagram of monostable multivibrator using 555timer and derive an expression for its frequency of oscillation.	Evaluate	5
7	Derive the expression for i) capture range in PLL ii) Lock in range in PLL.	Analyze	6
8	Draw the circuit of a 1st order band pass filter and derive its transfer function.	Analyze	4
9	Draw the circuit of a all pass filter and derive its transfer function.	Analyze	4
10	Derive the voltage to frequency converter factor for VCO.	Analyze	6
11	Explain any two applications of Astable multivibrator using 555IC.	Analyze	5
12	Explain VCO operation in PLL.	Understand	6
13	Explain triangular waveform generator using IC 741	Understand	5
14	Design second order high pass filter.	Evaluate	4
15	Derive the frequency of oscillations in VCO.	Analyze	6
ANALYTICAL QUESTIONS			
1	Design an Astable Multivibrator using 555 Timer to produce 1Khz square wave form for duty cycle=0.50	Evaluate	5
2	Design and draw the wave forms of 1KHZ square waveform generator using555 Timer for duty cycle D=25% .	Evaluate	5
3	Design a 555 based square wave generator to produce an asymmetrical square wave of 2 KHz. If Vcc=12V, draw the voltage curve across the timing capacitor and output waveform.	Analyze	5
4	Draw the schematic diagram of an all pass filter and determine the phase shift φ between the input and output at f = 2kHz.	Analyze	4
5	Design a HPF at a cutoff frequency of 1 KHz and a pass band gain of 2.	Analyze	4
6	Design a LPF at a cutoff frequency of 1 KHz and a pass band gain of 2.	Analyze	4
7	Design a 2^{nd} order HPF at a cutoff frequency of 2 KHz.	Analyze	4
7	Design a 2^{nd} order LPF at a cutoff frequency of 4 KHz.	Analyze	4
8	Compute the cutoff frequency for 1^{st} order HPF, if R = 10K ohms and C = 0.02μF.	Analyze	4
9	Design 1^{st} order wideband pass filter if lower cut off frequency is 500Hz, and upper cut off frequency is 2KHz.	Analyze	4
10	Compute the cutoff frequency for 1^{st} order LPF, if R = 5K ohms and C =	Analyze	4

	0.01μF.		
11	Design 1st order wideband pass filter if lower cut off frequency is 1000Hz, and upper cut off frequency is 4KHz.	Analyze	4
12	Design a square wave generator of frequency 100Hz and duty cycle of 50%.	Evaluate	5
13	Determine the dc control voltage V_c at lock if signal frequency f_s = 10 KHz, VCO free running frequency is 10.66KHz and the voltage to frequency transfer coefficient of VCO is 6600 Hz/V.	Analyze	6
14	Calculate output frequency f_0 , lock range and capture range of a 565 PLL if RT = 10K ohms, CT = 0.01μF and C = 10 μF.	Analyze	6
15	Design a square wave generator of frequency 100Hz and duty cycle of 75%.	Evaluate	5
	UNIT-3 **DATA CONVERTERS** **SHORT ANSWER QUESTIONS**		
1	Define data converters?	Remember	8
2	Indicate types of data converters.	Remember	8
3	Name the different DAC techniques.	Remember	8
4	Define weighted resistor type DAC.	Understand	8
5	Sketch the 2 bit weighted resistor type DAC.	Understand	8
6	Sketch the 3 bit weighted resistor type DAC.	Understand	8
7	Sketch the 4 bit weighted resistor type DAC.	Understand	8
8	Define R-2R Ladder DAC.	Understand	8
9	Sketch the 2 bit R-2R Ladder DAC.	Understand	8
10	Sketch the 3 bit R-2R Ladder DAC.	Understand	8
11	Sketch the 4 bit R-2R Ladder DAC.	Remember	8
12	Define inverted R-2R DAC.	Understand	8
13	Sketch the 2 bit inverted R-2R DAC.	Understand	8
14	Sketch the 3 bit inverted R-2R DAC.	Understand	8
15	Sketch the 4 bit inverted R-2R DAC.	Understand	8
16	Write the need of data converters.	Understand	8
17	Give applications of data converters.	Understand	8
18	Give the drawbacks of weighted resistor type DAC.	Understand	8
19	Give the advantages of weighted resistor type DAC.	Understand	8
20	Calculate basic step of 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output produced if the input is 101101111?	Apply	8
21	Calculate the values of the LSB output for an 8 bit DAC for the 0 to 10V range.	Analyze	8
22	How many levels are possible in a two bit DAC what is its resolution if the output range is 0 to 3V.	Apply	8
23	Calculate the values of the MSB output for an 8 bit DAC for the 0 to 10V range.	Apply	8
24	Calculate the values of the full scale output for an 8 bit DAC for the 0 to 10V range.	Apply	8
25	What output voltage would be produced by monolithic DAC whose output range is 0 to 10V and whose input binary is 10?	Analyze	8
26	What output voltage would be produced by monolithic DAC whose output range is 0 to 10V and whose input binary is 0110?	Analyze	8
27	What output voltage would be produced by monolithic DAC whose output range is 0 to 10V and whose input binary is 10111100?	Analyze	8
28	Define linearity error in DAC.	Remember	8
29	Define off set error in DAC.	Remember	8
30	Define resolution in DAC.	Remember	8
31	List the broad classification of ADCs	Remember	8
32	List out the direct type ADCs	Understand	8
33	Explain in brief the principle of operation of successive Approximation	Analyze	8

	ADC.		
34	What are the main advantages of integrating type ADCs?	Understand	8
35	What is the main drawback of a dual-slop ADC?	Remember	8
36	Define conversion time.	Remember	8
	LONG ANSWER QUESTIONS		
1	Explain the working of a Weighted resistor D/A converter.	Evaluate	8
2	Explain successive approximation A/D converter.	Understand	8
3	Explain the working of a dual slope A/D converter.	Remember	8
4	With neat diagram, explain the working principle of inverter R-2R ladder DAC.	Understand	8
5	Explain the working of a counter type A/D converter and state it's important feature.	Understand	8
6	Write the specifications of DAC.	Understand	8
7	Write the specifications of ADC.	Analyze	8
8	With neat diagram, explain the working principle of R-2R ladder type DAC.	Analyze	8
9	Explain the operation of parallel comparator type ADC.	Analyze	8
10	Design 4 bit weighted resistor DAC.	Analyze	8
	ANALYTICAL QUESTIONS		
1	A dual slope ADC uses a16-bit counter and a 4MHz clock rate. The maximum input voltage is+10v. The maximum integrator output voltage should be-8v when the counter has cycled through 2n counts. The capacitor used in the integrator is 0.1 µF Find the value of the resistor R of the integrator.	Apply	7,8
2	Find the voltage at all nodes 0, 1, 2, …. And at the output of a 5-bit R-2R ladder DAC. The least Significant bit is 1 and all other bits are equal to 0. Assume VR = -10V and R=10KΩ.	Remember	7,8
3	A dual slope ADC uses an 18 bit counter with a 5MHz clock. The maximum integrator input voltage in +12V and maximum integrator output voltage at 2n count is -10V. If R=100KO, find the size of the capacitor to be used for integrator.	Understand	7,8
4	Calculate basic step of 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output produced if the input is 101101111.	Apply	7,8
5	Calculate the values of the LSB,MSB and full scale output for an 8 bit DAC for the 0 to 10V range.	Apply	7,8
6	An ADC converter has a binary input of 0010 and an analog output of 20mv. What is the resolution.	Apply	7,8
7	How many levels are possible in a two bit DAC what is its resolution if the output range is 0 to 3V.	Apply	7
8	Find V(1)=5V what is the maximum output voltage.	Remember	7
9	Calculate what is the conversion time of a 10 bit successive approximation A/D converter if its 6.85V.	Apply	7
10	A dual slope uses a 16 bit counter and a 4 MHz clock rate. The maximum input voltage is +10V. The maximum integrator output voltage should be -8V when the counter has cycled through 2n counts. The capacitor used in the integrator is 0.1µf. Find the value of the resistor R of the integrator.	Apply	7
	UNIT-IV **DIGITAL INTERAGETED CIRCUITS** **SHORT ANSWER QUESTIONS**		
1	Write short notes on MOS transistors.	Remember	9
2	Design CMOS transistor circuit for 2-input AND gate.	Understand	9
3	Explain sourcing current of TTL output?	Remember	9
4	Which of the parameters decide the fan-out and how?	Understand	9
5	Explain sinking current of TTL output?	Understand	10

6	Explain the term Voltage levels for logic '1' & logic '0' with reference to TTL gate.	Understand	10
7	Explain the DC Noise margin with reference to TTL gate?	Understand	10
8	Explain Low-state unit load with reference to TTL gate?	Remember	10
9	Explain High-state fan-out with reference to TTL gate?	Remember	10
10	Explain the use of Package?	Remember	10
11	State the effect of loading CMOS output.	Understand	11
12	Explain with neat diagram interfacing of TTL gate driving CMOS gates.	Remember	11
13	What is combinational logic.	Remember	11
14	Write a short note on priority encoder.	Remember	11
15	What is multiplexer.	Understand	11
LONG ANSWER QUESTIONS			
1	Explain the following terms with reference to CMOS logic. i. Logic Levels ii. Noise margin iii. Power supply rails iv. Propagation delay	Apply	10
2	Draw the circuit diagram of two-input 10K ECL OR gate and explain its operation.	Analyze	11
3	Design CMOS transistor circuit for 2-input AND gate. Explain the circuit with the help of function table?	Remember	11
4	Draw the resistive model of a CMOS inverter circuit and explain its behavior for LOW and HIGH outputs.	Remember	11
5	Design a three input NAND gate using diode logic and a transistor inverter? Analyze the circuit with the help of transfer characteristics.	Evaluate	11
6	Realize the logic function performed by 74×381 with ROM.	Evaluate	11
7	Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.	Apply	11
8	Design combinational circuit for common anode 7 segment display / driver.	Apply	11
9	Design 16 bit adder using two 7483 ICs.	Remember	10
10	Explain sinking current and sourcing current of TTL output? Which of the parameters decide the fan-out and how?	Remember	10
11	Draw and explain the 2 input TTL NOR gate.	Understand	11
12	Draw the CMOS circuit diagram of tri-state buffer. Explain circuit with the help of logic diagram and function table.	Remember	11
13	Draw the circuit for CMOS OR-AND invert logic gates and explain its functioning.	Apply	11
14	Explain the operation of encoders.	Apply	12
15	Explain magnitude comparators.	Apply	12
ANALYTICAL QUESTIONS			
1	Analyze the fall time of CMOS inverter output with RL = 100, VL = 2.5V and CL=10PF. Assume VL as stable state voltage.	Analyze	11
2	Design a CMOS transistor circuit with the functional behavior f(X) = ((A+B')(B+D')(A+D'))'	Analyze	11
3	Design BCD to gray code converter.	Understand	11
4	Implement the following function with 8 : 1 MUX. F(W,X,Y,Z) = ∑m (2,4,6,7,10,11,12,13,14)	Analyze	11
5	Implement the following multi output combinational logic circuit using 4:16 decoder IC , AND external gates. F1 = ∑m (1,5,8,11) F2 = ∑m (1,6,8,9,12) F3 = ∑m (7,10,15)	Analyze	11
6	A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case?	Analyze	11
7	Design 4 bit comparator using IC7485	Understand	11
8	Design 8 bit comparator using two 7485 ICs.	Understand	11

9	Design look ahead carry generator using IC 74182.	Understand	11
10	Show the construction of 4 bit parallel adder using IC 74182.	Understand	11
11	Implement the following function with 8 : 1 MUX. F(W,X,Y,Z) = ∑m (0,1,3,5,8,9,15)	Analyze	11
12	Implement the following multi output combinational logic circuit using 4:16 decoder IC , AND external gates. F1 = ∑m (2,3,9,11) F2 = ∑m (10,12,13,14) F3 = ∑m (2,4,8)	Analyze	11
13	Design a 4:16 decoder using two 74X138 ICs.	Analyze	11
14	Realize the following expression using 74X151 IC	Analyze	11
15	Realize the following expression using 74X151 IC F(Y) = AB+BC+AC	Analyze	11
	UNIT-V **SEQUNTIAL LOGIC ICS AND MEMORIES** **SHORT ANSWER QUESTIONS**		
1	Define static RAM	Understand	13
2	Define dynamic RAM	Understand	13
3	Classify types of ROMs	Understand	13
4	What is the difference between latch& Flip-Flop,Explain with logic diagram.	Remember	12
5	Explain any one application of SR latch.	Understand	12
6	What is race around condition? How it is avoided?	Remember	12
7	How synchronous counters differ from asynchronous counters?	Understand	12
8	List counter applications.	Understand	12
9	What do you mean by sequential circuit? Explain with the help of block diagram.	Remember	12
10	Draw and explain the working of master slave JK flip-flop.	Understand	12
11	Covert JK flip-flop into T flip-flop.	Understand	12
12	Explain the working of 4 bit asynchronous counter.	Remember	12
13	List the basic types of shift registers interns of data movement.	Understand	12
14	Draw and explain the operation of controlled buffer register.	Understand	12
15	Draw and explain 4 bit Johnson counter.	Remember	12
	LONG ANSWER QUESTIONS		
1	How many ROM bits are required to build a 16-bit adder/subtractor with mode control, carry input, carry output and two's complement overflow out-put. Show the block schematic with all inputs and outputs.	Understand	13
2	Draw the basic cell structure of Dynamic RAM. What is the necessity of refresh cycle? Explain the timing requirements of refresh operation.	Analyze	13
3	Discuss in detail ROM access mechanism with the help of timing waveforms.	Analyze	13
4	Draw the logic diagram of 74×163 binary counter and explain its operation.	Understand	13
5	Design a modulo-100 counter using two 74×163 binary counters?	Apply	13
6	Design a Modulo-12 ripple counter using 74×74?	Apply	13
7	Discuss how PROM, EPROM, EEPROM technologies differ from each other?	Analyze	13
8	Differentiate between ripple counter and synchronous counter? Design a 4-bit counter in both modes and estimate the propagation delay.	Remember	13
9	Design a modulo-88 counter using 74X163 Ics.	Understand	13
10	Draw the logic diagram of 74×163 binary counter and explain its operation.	Remember	11
	ANALYTICAL QUESTIONS		
1	Determine the ROM size needed to realize the logic function performed by 74×153 and 74×139.	Apply	13
2	Realize the logic function performed by 74×381 with ROM.	Evaluate	13
3	Explain the internal structure of 64K×1 DRAM with the help of timing diagrams.	Apply	13

4	Explain the necessity of two-dimensional decoding mechanism in memories. Draw MOS transistor memory cell in ROM and explain the operation.	Apply	13
5	Design excess-3 decimal counter using 74X163.	Apply	12
6	How many flip-flops are required to build a binary counter that counts from 0 to 1023. And draw binary counter.	Apply	12
7	Design a 4 bit, 4 state ring counter using 74X194.	Apply	12
8	Design a 4 bit, 8 state Johnson counter using 74X194.	Apply	12
9	Explain the operation of a D latch through suitable timing diagrams for various possibilities of input.	Apply	13
10	Design an 8 X 4 diode ROM using 74X138 for the following data starting from the first location. 1,4,9,B,A,O,F,C.	Apply	13
11	Design an 8 bit parallel –in and parallel-out shift register and explain the operation.	Apply	12
12	Design SR flip-flop and explain function.	Apply	12
13	Design negative edge triggered SR flip-flop	Understand	12
14	How many flip-flops are required to build a binary counter that counts from 0 to 256. And design the binary counter.	Apply	12
15	Design negative edge triggered D flip-flop.	Understand	12

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Date: 12th July, 2017

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