INSTITUTE OF AERONAUTICAL ENGINEERING

(**Autonomous**)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Name	:	**COMPUTER ARCHITECTURE**
Course Code	:	**BES003**
Class	:	M. Tech ISemester
Branch	:	EMBEDDED SYSTEMS
Year	:	2017 – 2018
CourseCoordinator	:	Manisha Guduri, Assistant professor Department of ECE
Course Faculty	:	Mr. M.Bhargav Kumar, Assistant Professor, Department of ECE

I. COURSE OBJECTIVES:

The course should enable the students to:

S. No	Description
I	Acquire knowledge of electrical characteristics of ideal and practical diodes under forward and reverse bias to analyze and design diode application circuits such as rectifiers and voltage regulators.
II	Utilize operational principles of bipolar junction transistors and field effect transistors to derive appropriate small-signal models and use them for the analysis of basic amplifier circuits.
III	Perform DC analysis (algebraically and graphically using current, voltage curves with superimposed load line) and design of CB, CE and CC transistor circuits.
IV	Compare and contrast different biasing and compensation techniques.

II. COURSE LEARNING OUTCOMES:

Students who complete the course will have demonstrated the ability to do the following

CAEC001.01	Understand and analyze different types of diodes, operation and its characteristics in order to design basic circuits.
CAEC001.02	Design full wave rectifier without filter and different filters for the given specifications.
CAEC001.03	Explain the operational characteristics of various special purpose diodes such as zener diode, Tunnel diode, varactor diode and photo diode.
CAEC001.04	Explain half wave rectifier without filter and with different filters for the given specifications.
CAEC001.05	Write Use of diodes in typical circuits: rectifiers, regulated power supplies, limiting circuits.
CAEC001.06	Understand the different parameters of transistors such as depletion width and channel width for understanding the functioning and design of this component.
CAEC001.07	Estimate the performance of BJTs on the basis of their operation and working.
CAEC001.08	Distinguish the constructional features and operation of FET and MOSFET and their applications.

CAEC001.09	Analyze the performance of FETs on the basis of their operation and working.
CAEC001.10	Develop the capability to analyze and design simple circuits containing non-linear elements such as transistors using the concepts of load lines, operating points and incremental analysis.
CAEC001.11	Identify the various transistor biasing circuits and its usage in applications like amplifiers.
CAEC001.12	Discuss and Design small signal amplifier circuits applying the various biasing techniques.
CAEC001.13	Explain basic circuits like dc and biasing circuits, small-signal ac circuits with emphasis on single-stage amplifiers.
CAEC001.14	Describe amplifier circuits, oscillators and filter circuits employing BJT, FET devices.
CAEC001.15	Construct, and take measurement of various analog circuits to compare experimental results in the laboratory with theoretical analysis.
CAEC001.16	Apply small-signal models to devices and determine the voltage gain and input and output impedances.
CAEC001.17	Acquire experience in building and trouble shouting simple electronic analog circuits.
CAEC001.18	Apply the concept of electronic devices and circuits to understand and analyze real time applications.
CAEC001.19	Acquire the knowledge and develop capability to succeed national and international level competitive examinations.

TUTORIAL QUESTION BANK

UNIT-I			
FUNDAMENTALS OF COMPUTER DESIGN			
PART – A (SHORT ANSWER QUESTIONS)			
S. No	**QUESTION**	**Blooms Taxonomy level**	**Course Learning Outcomes**
1	Define AmDahl's Law.	Remember	CBES003.01
2	Define computer architecture	Understand	CBES003.01
3	Explain addressing modes for signal processing.	Understand	CBES003.01
4	Classify memory addressing	Understand	CBES003.01
5	What is cost measuring and reporting performance.	Understand	CBES003.01
6	Explain operations in Instruction set.	Remember	CBES003.01
7	What are quantitative principles of computer design	Remember	CBES003.01
8	Explain about trends related to Power and Energy.	Remember	CBES003.01
9	How to encode an instruction set?	Remember	CBES003.01
10	Explain the instructions for control flow.	Remember	CBES003.01
11	What are the trends in technology?	Understand	CBES003.01
12	Define Measuring and reporting performances	Remember	CBES003.01

13	Explain about Instruction set architecture (ISA) design	Remember	CBES003.01
14	List the types of computers.	Remember	CBES003.01
15	Explain the role of compiler.	Understand	CBES003.03
16	Define compiler.	Remember	CBES003.01
PART – B (LONG ANSWER QUESTIONS)			
1	What are the trends in technology related to power, energy and cost? How do you evaluate the Performance?	Remember	CBES003.01
2	What are the trends in technology? Explain performance trends bandwidth over latency.	Analyze	CBES003.01
3	Design the organization and hardware to meet goals and functional requirements of computer architecture.	Understand	CBES003.01
4	Find the die yield for dies that are 1.5cm on a side and 1.0cm on a side, assuming a defect density of 0.4 per cm^2 and α is 4.	Remember	CBES003.01
5	List out various instructions for flow control and the supporting addressing modes? What are the parameters of evaluation?	Understand	CBES003.01
6	Define performance. Describe how the five levels of programs are used in evaluating performance	Remember	CBES003.01
7	How Amdahl's law is useful for measurement of improved performance of computer systems	Understand	CBES003.03
8	Classify memory addressing. Explain the addressing modes for instruction set architecture.	Understand	CBES003.01
9	Describe the type and size of operands in set architecture. Explain the operations in the instruction set.	Understand	CBES003.01
10	Find the number of dies per 300mm (30cm) wafer for a die that is 1.5cm on a side. The die area is 2.25cm^2.	Understand	CBES003.01
11	Define compiler. Explain the role of compiler in detail.	Understand	CBES003.03
12	Define instruction cycle. Explain about Instruction set architecture (ISA) design	Remember	CBES003.01
UNIT-II			
INSTRUCTION LEVEL PARALLELISM			
PART - A (SHORT ANSWER QUESTIONS)			
1	What is instruction level parallelism?	Remember	CBES003.14
2	Discuss ILP using dynamic scheduling.	Remember	CBES003.03
3	Discuss the use of compiler in achieving ILP?	Understand	CBES003.03
4	What are the limitations of ILP.	Remember	CBES003.03
5	Explain VLIW approach.	Understand	CBES003.03
6	Define static branch protection.	Understand	CBES003.03

7	Explain instruction delivery.	Understand	CBES003.01
8	Explain compiler techniques.	Understand	CBES003.01
9	Define data dependences.	Remember	CBES003.01
10	Define data hazards.	Remember	CBES003.04
11	Explain pipeline scheduling.	Remember	CBES003.04
12	Define multithreading.	Remember	CAEC001.04
13	Define an ideal processor or perfect processor.	Remember	CAEC001.02
14	What is the impact of speculation on energy efficiency?	Understand	CAEC001.02
15	Write about Speculation through Multiple Branches	Understand	CAEC001.02
PART– B (LONG ANSWER QUESTIONS)			
1	What is instruction level parallelism? Elaborate instruction level parallelism concepts and challenges.	Understand	CAEC001.05
2	Explain basic compiler techniques for exposing ILP with basic pipeline scheduling and loop unrolling.	Remember	CAEC001.04
3	Show how the loop would look on IMPS, both scheduled and unscheduled, including nay stalls or idle clock cycle. Schedule for delays from floating-point operations, but remember that we are ignoring delayed branches.	Remember	CAEC001.02
4	Discuss ILP using dynamic scheduling, multiple issue and speculation with one example.	Understand	CAEC001.02
5	Describe the compiler techniques, static branch protection and VLIW approach? What are the limitations of ILP.	Understand	CAEC001.02
6	Discuss the use of compiler in achieving ILP? What are the issues involved and how to overcome them?	Understand	CAEC001.02
7	A non pipeline system takes 50ns to process a task. The same task can be proceed in a six-segment pipeline with a clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved.	Remember	CAEC001.02
8	A magnetic disk has the following parameters: Ts = Average time to position the magnetic head over a track, R = Rotation speed of disk in revolutions per second,Nt = Number of bits per track,Ns = Number of bits per sector. Calculate the average time Ta that it will take to read one sector.used with a Full Wave filter?	Understand	CAEC001.02
9	Explain about Reducing Branch Costs with Advanced Branch Prediction.	Remember	CAEC001.02 CAEC001.02
12	Explain about Overcoming Data Hazards with Dynamic Scheduling.	Understand	CAEC001.02
13	Discuss about Advanced Techniques for Instruction Delivery and Speculation.	Understand	CAEC001.02 CAEC001.02
14	Describe the assumptions made for an ideal processor or perfect processor.	Remember	CAEC001.02

UNIT-III			
MEMORY HIERARCHY DESIGN			
PART –A (SHORT ANSWER QUESTIONS)			
1	Explain multiprocessor cache coherence?	Remember	CAEC001.06
2	How do you encode an instruction?	Understand	CAEC001.06
3	What is the use of virtual memory?	Understand	CAEC001.06
4	Write short notes on symmetric shared memory architectures	Understand	CAEC001.06
5	Write short notes on multiprocessor cache coherence	Understand	CAEC001.06
6	Define virtual memory.	Understand	CAEC001.06
7	Write an example on virtual memory.	Remember	CAEC001.06
8	Explain reducing cache misses penalty.	Remember	CAEC001.06
9	Write short notes on synchronization.	Understand	CAEC001.06
10	Explain about multithreading.	Remember	CAEC001.06
11	Explain snooping protocols.	Understand	CAEC001.06
12	List out the limitations in Symmetric Shared-Memory Multiprocessors.	Understand	CAEC001.06
13	Discuss the performance of Symmetric Shared-Memory Multiprocessors.	Understand	CAEC001.06
14	Define Directory-Based Coherence	Remember	CAEC001.06
PART – B (LONG ANSWER QUESTIONS)			
1	Describe the protection and examples of virtual memory (VM) mapping with a neat diagram.	Understand	CAEC001.06
2	What is the use of virtual memory? Explain virtual memory mapping with a neat diagram.	Remember	CAEC001.06
3	Write notes on symmetric shared memory architectures and multiprocessor cache coherence.	Remember	CAEC001.06
4	What are the limitations of dynamically scheduled pipelines and how hardware based speculation can address these limitations?	Understand	CAEC001.06
5	Distinguish distributed shared memory and directory based cache coherence protocols with diagram.	Evaluate	CAEC001.06
6	Explain about cache performance? How it can be improved?	Understand	CAEC001.06
7	Explain how to reduce cache miss penalty and miss rate.	Understand	CAEC001.06
8	Distinguish between symmetric shared memory and distributed shared memory architectures.	Evaluate	CAEC001.06
9	Explain about synchronization and multithreading.	Remember	CAEC001.06
10	Explain about directory based cache coherence protocols with diagram.	Remember	CAEC001.07

UNIT-IV			
STORAGE SYSTEMS			
PART – A (SHORT ANSWER QUESTIONS)			
1	What are the errors and failures in storage systems?	Remember	CAEC001.06
2	What is bench marking on a storage device?	Remember	CAEC001.06
3	Explain the concept of RAID.	Remember	CAEC001.06
4	Write short notes on Buses.	Remember	CAEC001.06
5	What are the effects of benchmarking.	Evaluate	CAEC001.06
6	Define reliability, availability and dependability	Remember	CAEC001.06
7	List and explain various RAID levels.	Understand	CAEC001.07
8	How to design an input/output system?	Remember	CAEC001.07
9	Explain how I/O devices are interfaced to CPU memory	Evaluate	CAEC001.14
10	Distinguish the real faults and failures in storage systems?	Understand	CAEC001.07
11	Define dependability.	Remember	CAEC001.07
12	Define Error latency.	Remember	CAEC001.07
PART – B (LONG ANSWER QUESTIONS)			
1	With a neat block diagram explain how I/O devices are interfaced to CPU memory, the storage system types and busses.	Remember	CAEC001.11
2	What are the errors and failures in storage systems? Discuss in detail with the errors and failures.	Understand	CAEC001.11
3	Discuss in detail with the concept of RAID and explain various levels and their applicability.	Remember	CAEC001.11
4	What is bench marking on a storage device? with this bench marking what are the effects it will occur on a storage device	Understand	CAEC001.11
5	Explain how the input/output (I/O) performance, reliability measures and bench marks.	Understand	CAEC001.11
6	Distinguish the real faults and failures in storage systems? Discuss in detail with the faults and failures.	Understand	CAEC001.11
7	Summarize the concept of Redundant Array of Independent Disk (RAID) and explain various levels and their applicability.	Remember	CAEC001.11
8	What is bench marking on a storage device? Distinguish between the crosscutting issues of block servers and filers	Remember	CAEC001.11
9	Discuss various levels of RAID and its importance in system maintenance.	Evaluate	CAEC001.11
10	Explain the reliability, availability and dependability.	Understand	CAEC001.10

11	Explain I/O subsystem in a dual processor system.	Remember	CAEC001.11
12	Define Bus. Explain different types of bus system.	Remember	CAEC001.11
UNIT-V			
INTER CONNECTION NETWORKS AND CLUSTERS			
PART – A (SHORT ANSWER QUESTIONS)			
1	Write about interconnection network media.	Remember	CAEC001.14
2	What are the practical issues in interconnecting networks.	Remember	CAEC001.12
3	Write about designing procedure of a cluster?	Remember	CAEC001.12
4	Design a cluster with an example in interconnection networks.	Remember	CAEC001.12
5	What is cluster?	Remember	CAEC001.12
6	Describe the advantages of clusters?	Remember	CAEC001.12
7	Explain the phases in cluster design process.	Remember	CAEC001.12
8	Explain about the transmission media.	Remember	CAEC001.12
9	Write an example for interconnection network media.	Remember	CAEC001.12
10	Explain the hierarchy of network media.	Remember	CAEC001.16
PART – B (LONG ANSWER QUESTIONS)			
1	Write about interconnection network media. How it will influence the networking media.	Remember	CAEC001.12
2	Elaborate the practical issues in interconnecting networks discuss in detail with few examples?	Remember	CAEC001.12
3	Illustrate the concepts of practical issues in interconnecting networks. How it will effect on a network media.	Understand	CAEC001.12
4	Interpret the designing procedure of a cluster. Design a cluster with an example in interconnection networks.	Understand	CAEC001.12
5	What is cluster? Describe the advantages of clusters?	Understand	CAEC001.12
6	Explain the transmission media used in inter connection networks.	Analyze	CAEC001.12
7	What is a cluster? Explain the process of designing clusters.	Understand	CAEC001.16
8	Describe the phases in cluster design process.	Remember	CAEC001.16
9	Explain the drawbacks of clusters.	Remember	CAEC001.16

HEAD OF THE DEPARTMENT
ELECTRONICS AND COMMUNICATION ENGINEERING